FIG.1

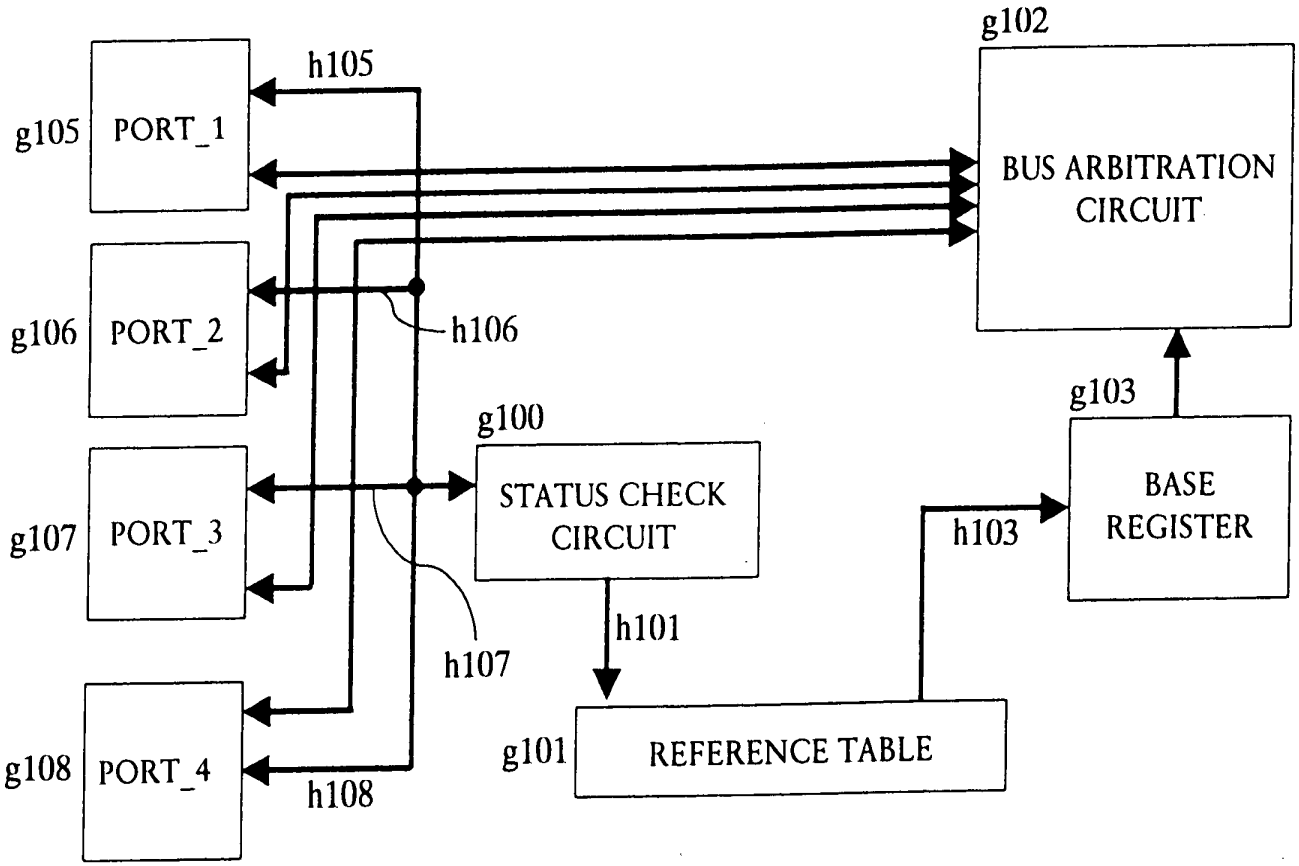

g102
BUS ARBITRATION CIRCUIT
h105
g105
PORT_1
g106
PORT_2
h106
g103
BASE REGISTER
g100
STATUS CHECK CIRCUIT
h103
g107
PORT_3
h101
h107
g108
PORT_4
h108
g101
REFERENCE TABLE

FIG. 2

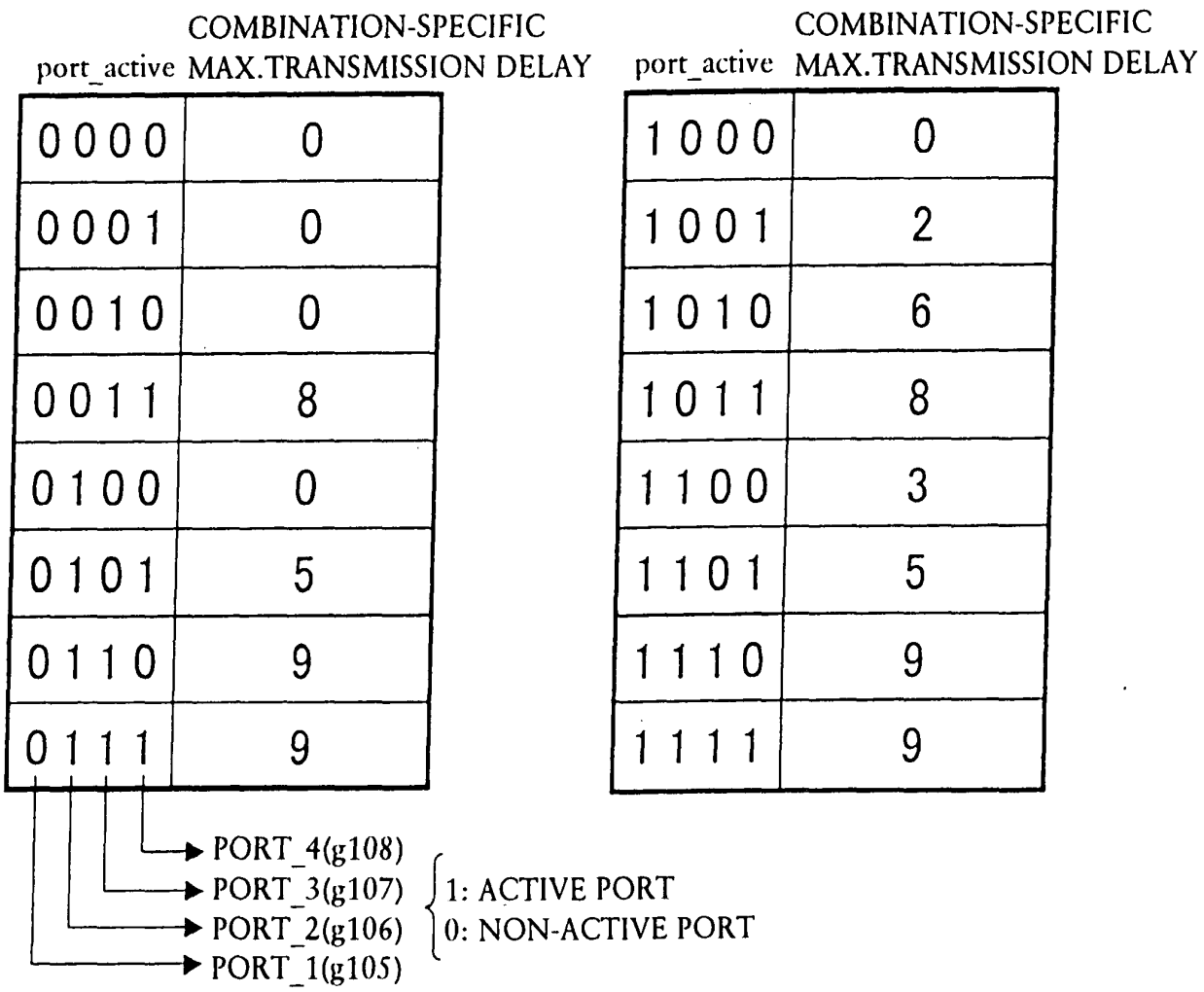

port_active
COMBINATION-SPECIFIC MAX.TRANSMISSION DELAY
0000 0
0001 0
0010 0
0011 8
0100 0
0101 5
0110 9
0111 9
port_active
COMBINATION-SPECIFIC MAX.TRANSMISSION DELAY
1000 0
1001 2
1010 6
1011 8
1100 3
1101 5
1110 9
1111 9
PORT_4(g108)
PORT_3(g107)
PORT_2(g106)
PORT_1(g105)
1: ACTIVE PORT
0: NON-ACTIVE PORT

FIG.3

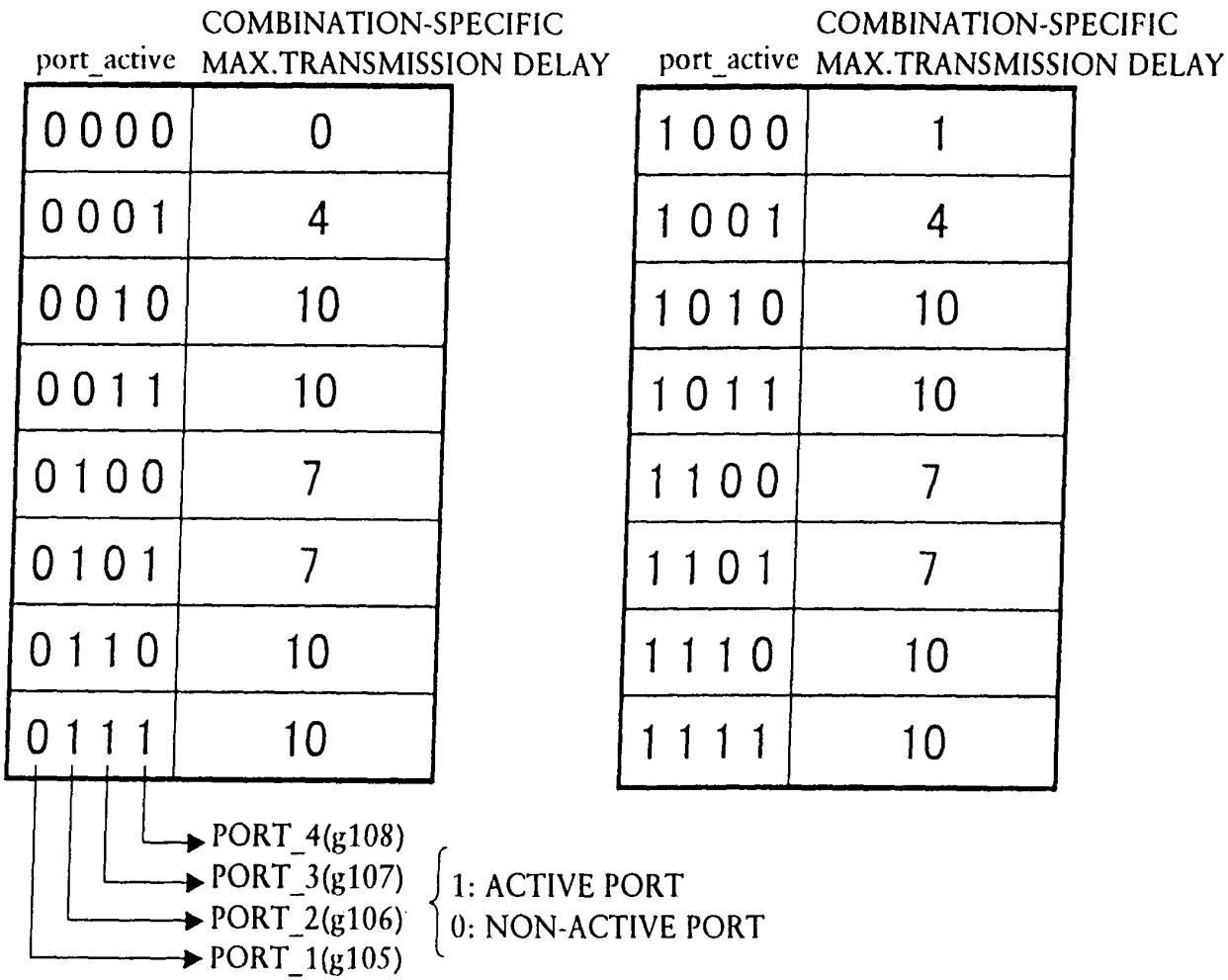

port_active
COMBINATION-SPECIFIC MAX.TRANSMISSION DELAY
0000 0
0001 4
0010 10
0011 10
0100 7
0101 7
0110 10
0111 10
port_active
COMBINATION-SPECIFIC MAX.TRANSMISSION DELAY
1000 1
1001 4
1010 10
1011 10
1100 7
1101 7
1110 10
1111 10
PORT_4(g108)
PORT_3(g107)
PORT_2(g106)
PORT_1(g105)
1: ACTIVE PORT
0: NON-ACTIVE PORT

FIG.4

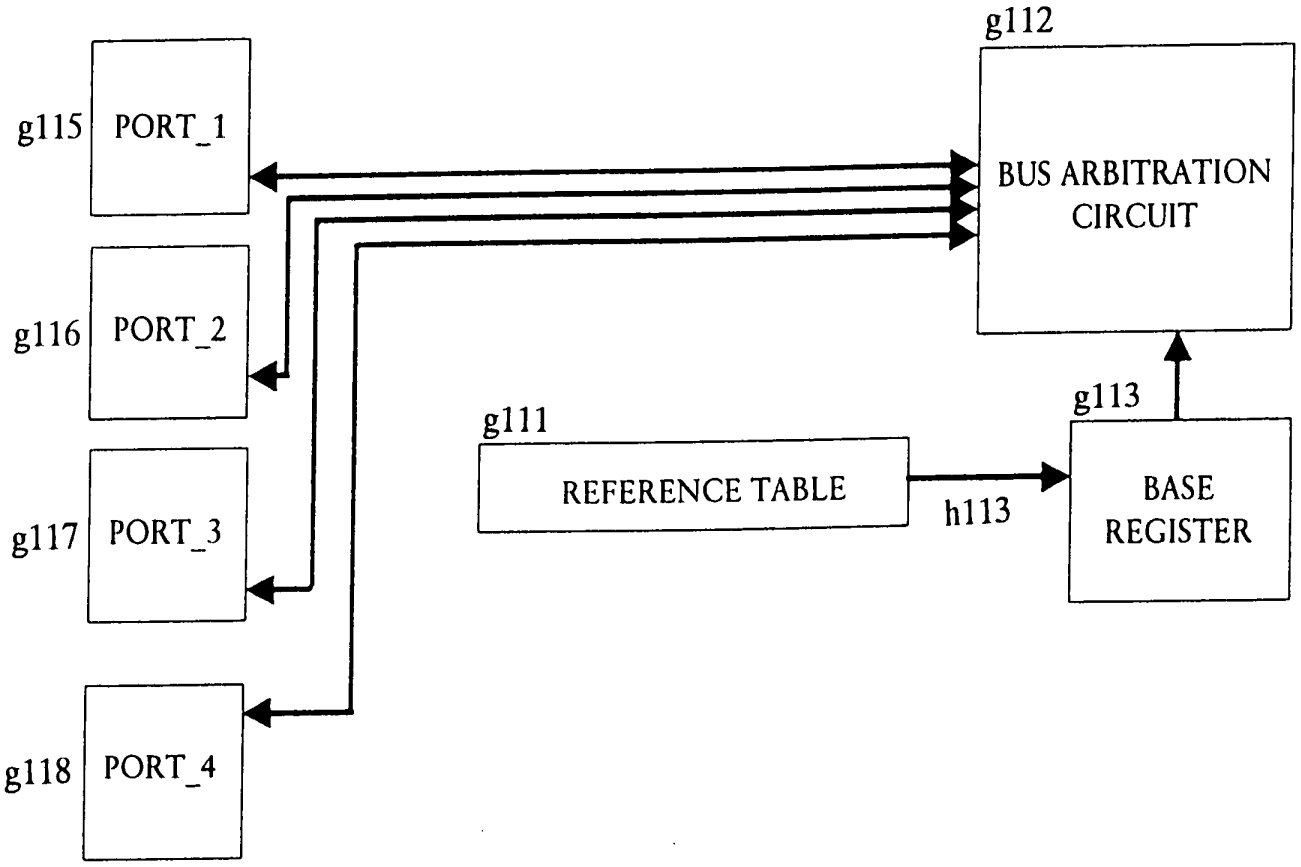

g112
BUS ARBITRATION CIRCUIT
g115
PORT_1
g116
PORT_2
g117
PORT_3
g118
PORT_4
g111
REFERENCE TABLE
h113
g113
BASE REGISTER

FIG.5

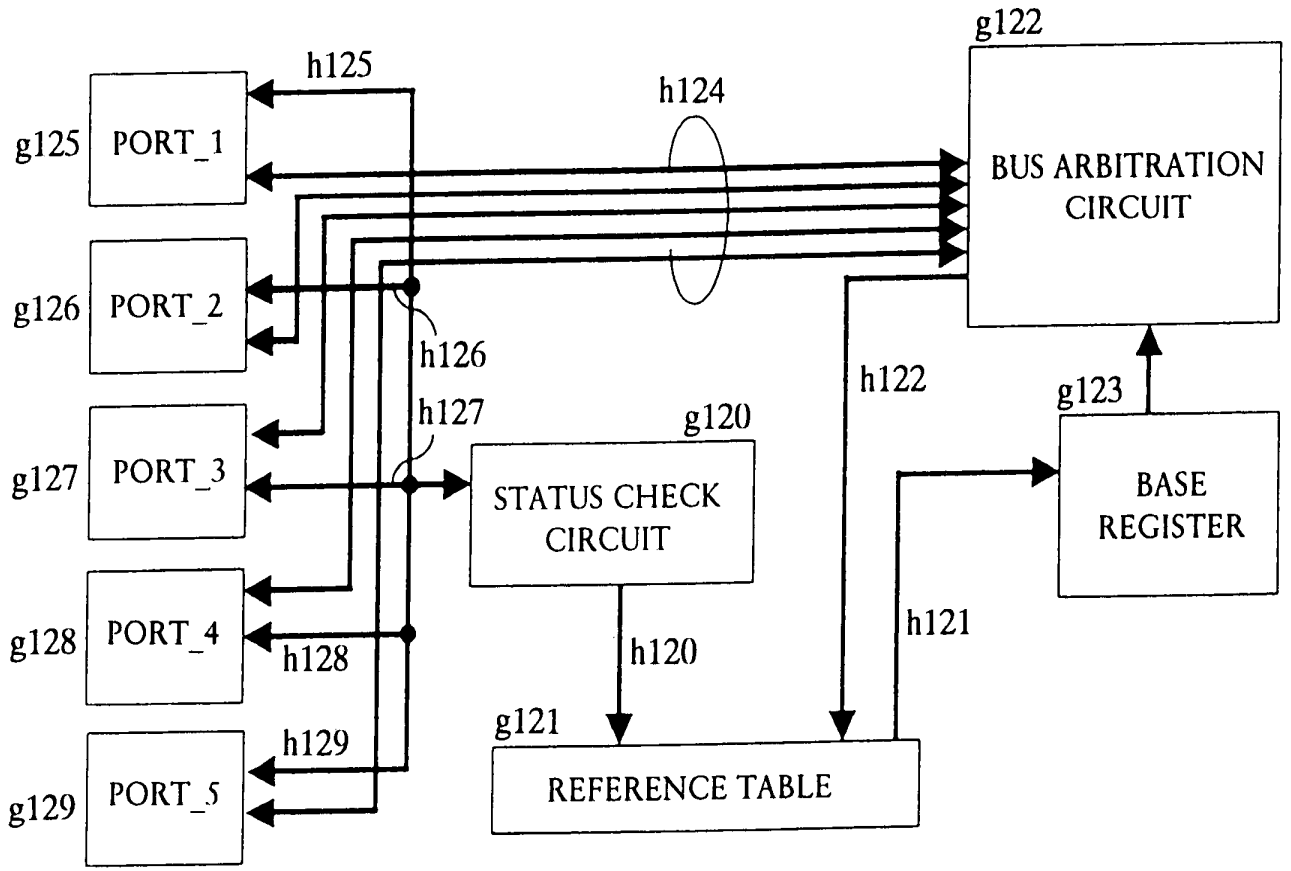

g122
h125
h124
g125
PORT_1
BUS ARBITRATION CIRCUIT
g126
PORT_2
h126
h122
h127
g123
g120
g127
PORT_3
STATUS CHECK CIRCUIT
BASE REGISTER
g128
PORT_4
h128
h120
h121
g121
h129
g129
PORT_5
REFERENCE TABLE

FIG.6

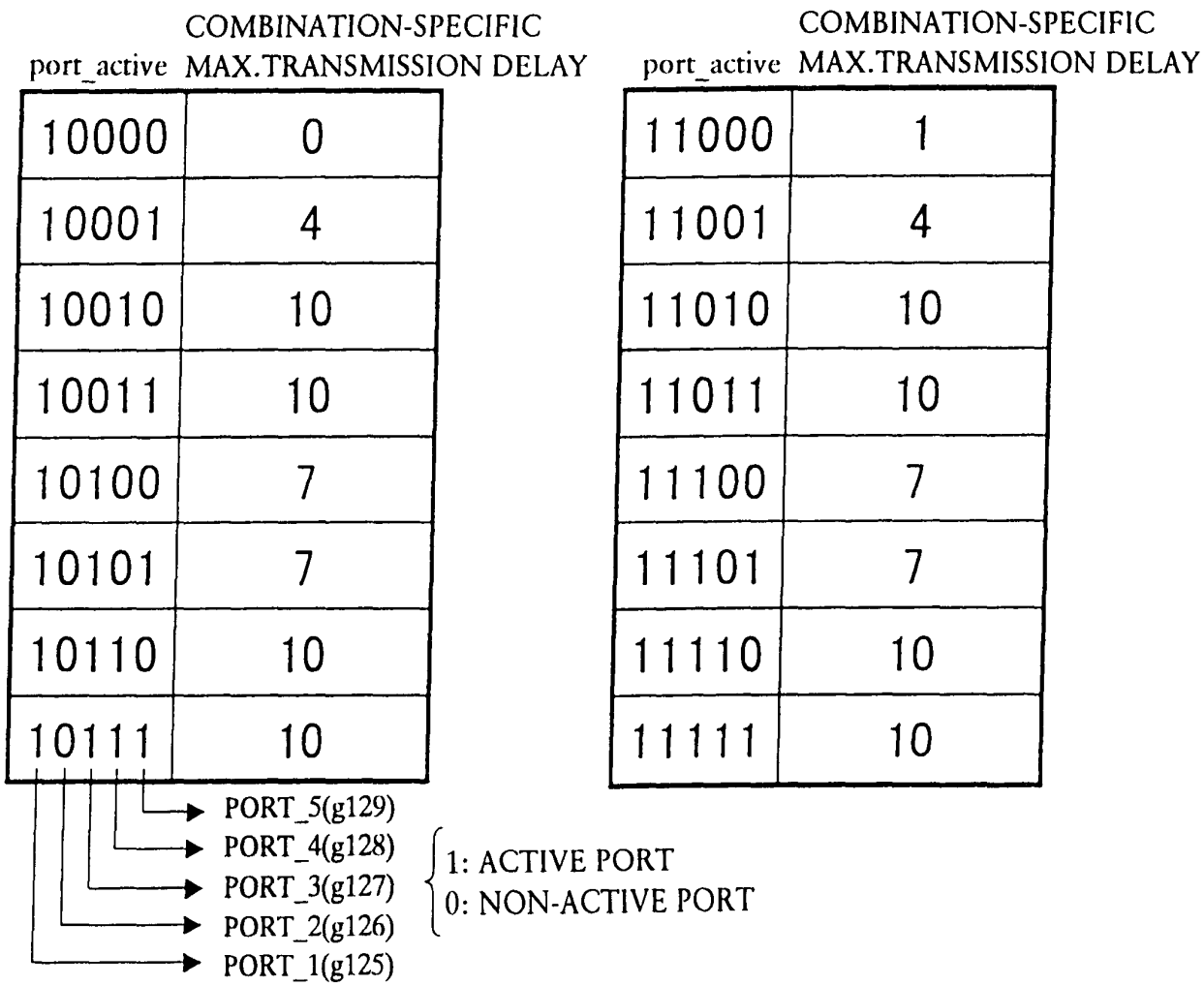

port_active
COMBINATION-SPECIFIC MAX.TRANSMISSION DELAY
10000 0
10001 4
10010 10
10011 10
10100 7
10101 7
10110 10
10111 10
port_active
COMBINATION-SPECIFIC MAX.TRANSMISSION DELAY
11000 1
11001 4
11010 10
11011 10
11100 7
11101 7
11110 10
11111 10
PORT_5(g129)
PORT_4(g128)
PORT_3(g127)
PORT_2(g126)
PORT_1(g125)
1: ACTIVE PORT
0: NON-ACTIVE PORT

FIG.7

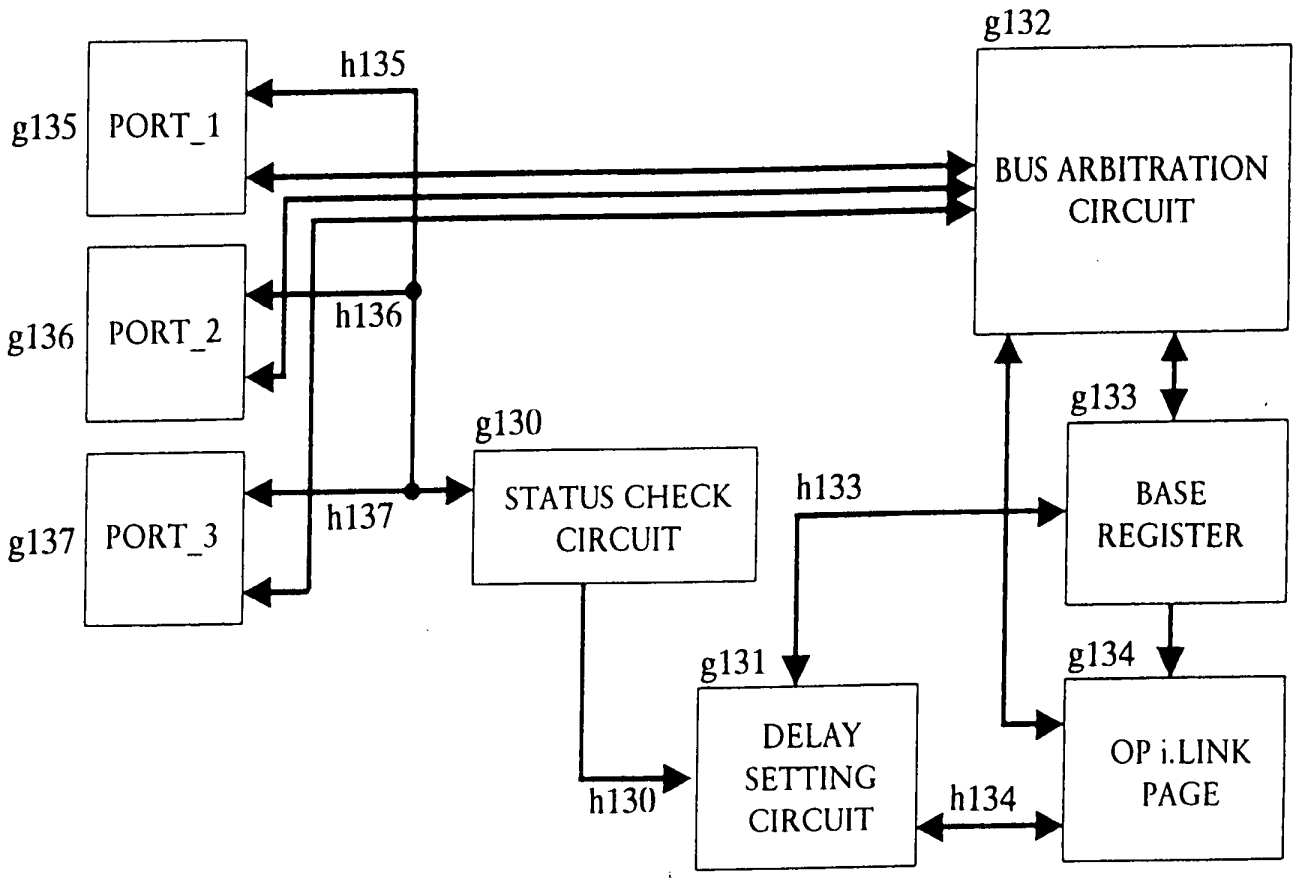

g132
h135
g135
PORT_1
BUS ARBITRATION CIRCUIT
g136
PORT_2
h136
g133
g130
STATUS CHECK CIRCUIT
h133
BASE REGISTER
g137
PORT_3
h137
g131
g134
DELAY SETTING CIRCUIT
OP i.LINK PAGE
h130
h134

FIG.8

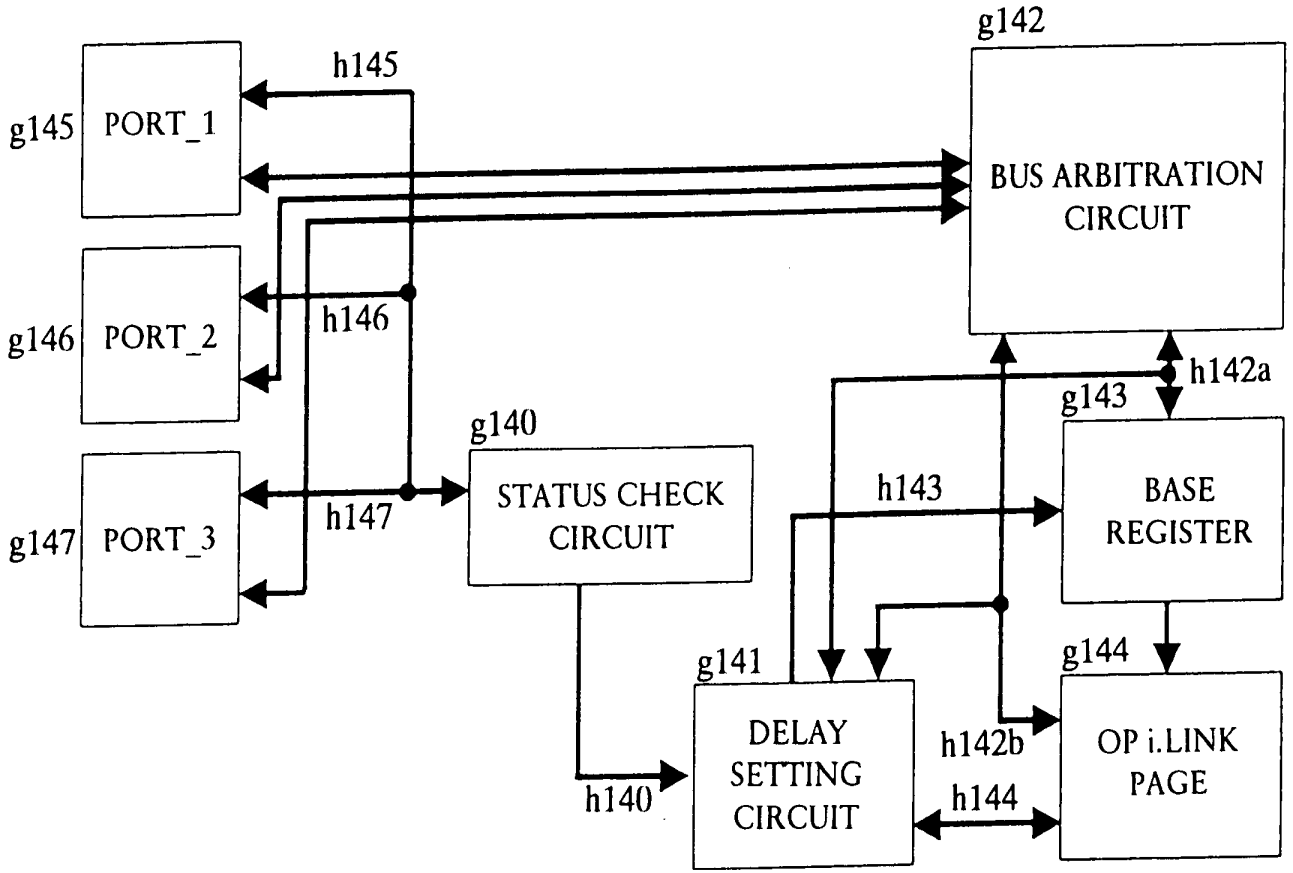

g142
h145
g145
PORT_1
BUS ARBITRATION CIRCUIT
g146
PORT_2
h146
h142a
g143
g140
STATUS CHECK CIRCUIT
h143
BASE REGISTER
g147
PORT_3
h147
g141
g144
DELAY SETTING CIRCUIT
h142b
OP i.LINK PAGE
h140
h144

FIG.9

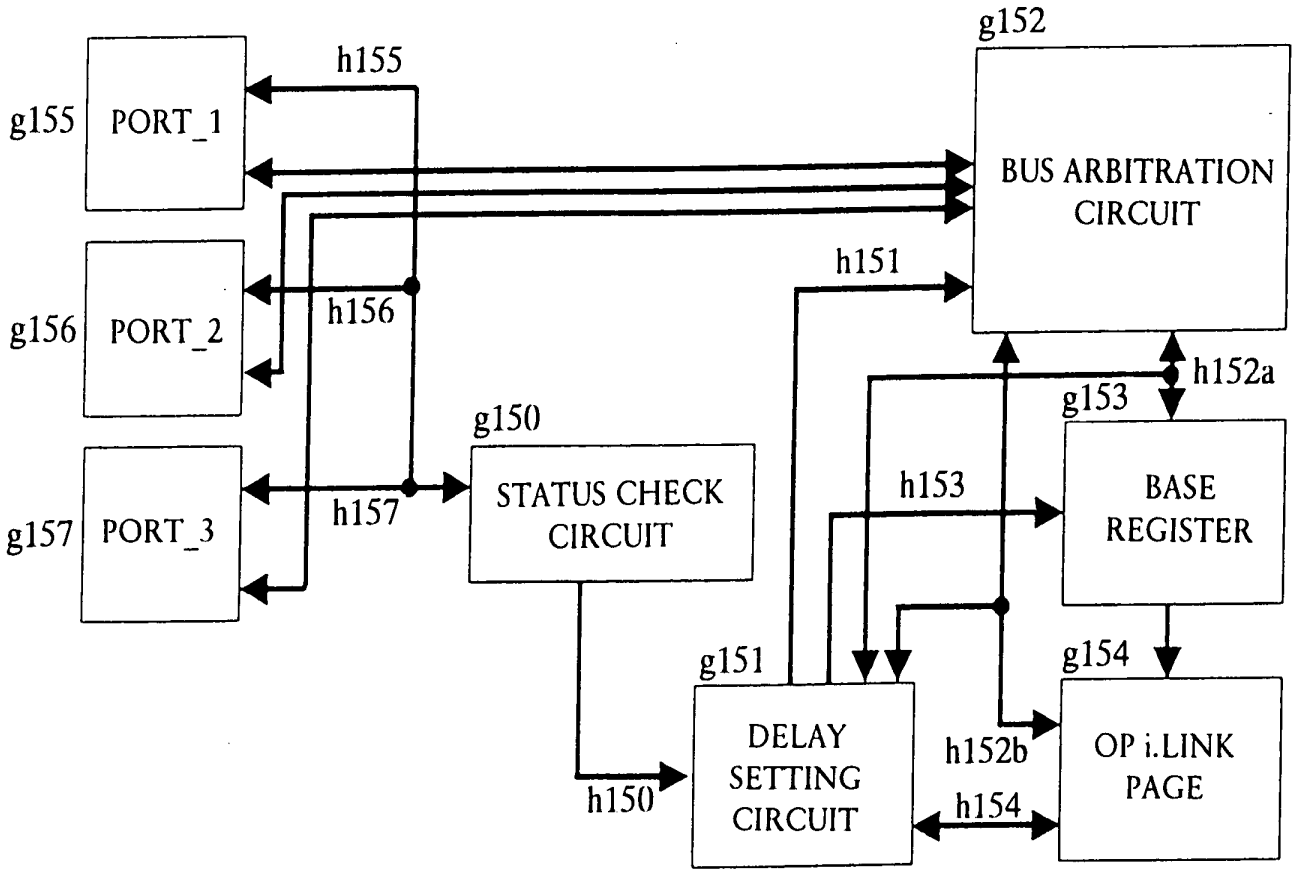

g152
h155
g155
PORT_1
BUS ARBITRATION CIRCUIT
h151
g156
PORT_2
h156
h152a
g153
g150
h153
BASE REGISTER
g157
PORT_3
h157
STATUS CHECK CIRCUIT
g151
g154
DELAY SETTING CIRCUIT
h152b
OP i.LINK PAGE
h150
h154

FIG.10

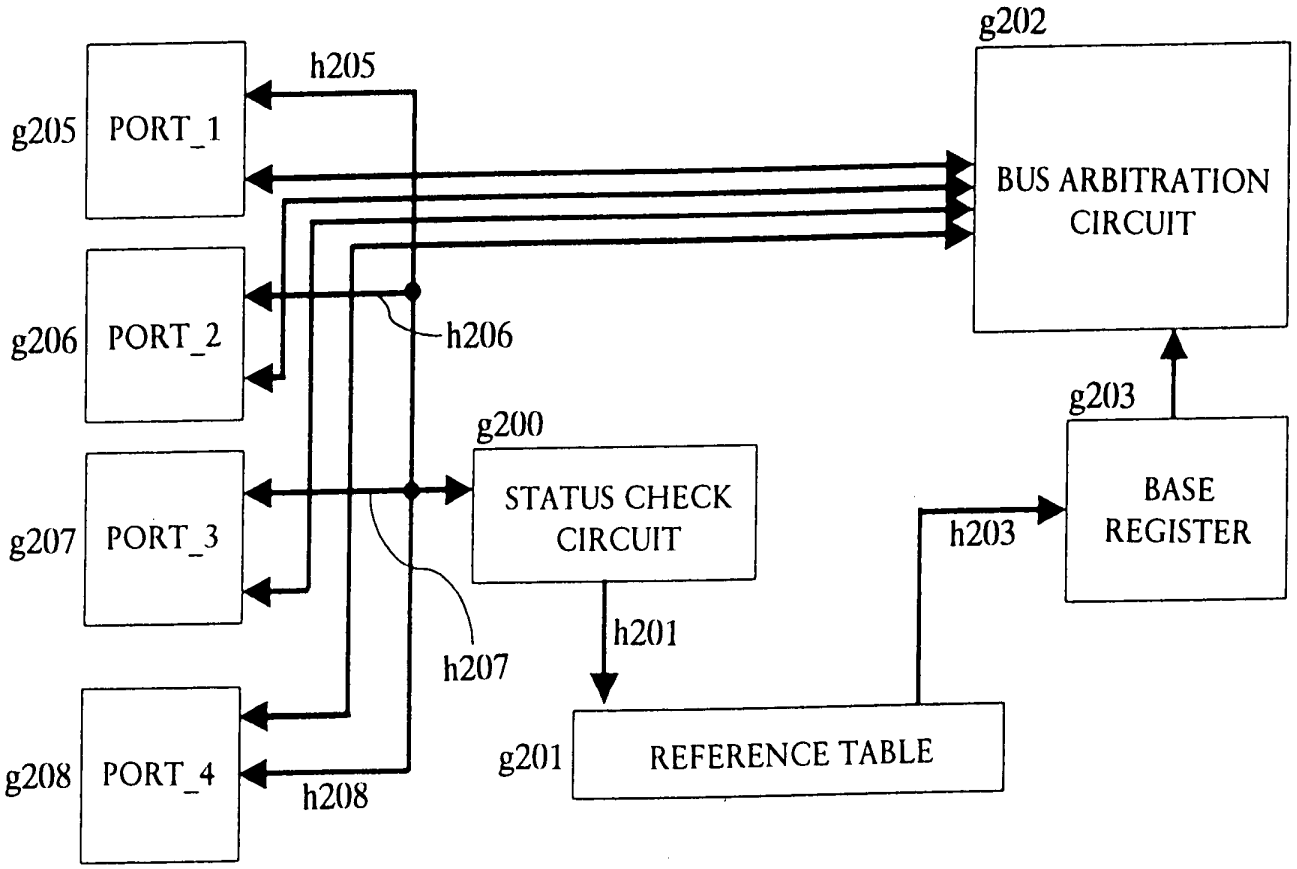

g202
BUS ARBITRATION CIRCUIT
h205
g205
PORT_1
g206
PORT_2
h206
g200
STATUS CHECK CIRCUIT
g203
BASE REGISTER
g207
PORT_3
h203
h201
h207
g208
PORT_4
h208
g201
REFERENCE TABLE

FIG.11

port_active	COMBINATION-SPECIFIC MAX.JITTER
0000	0
0001	0
0010	0
0011	3
0100	0
0101	5
0110	9
0111	9

port_active	COMBINATION-SPECIFIC MAX.JITTER
1000	0
1001	2
1010	6
1011	6
1100	3
1101	5
1110	9
1111	9

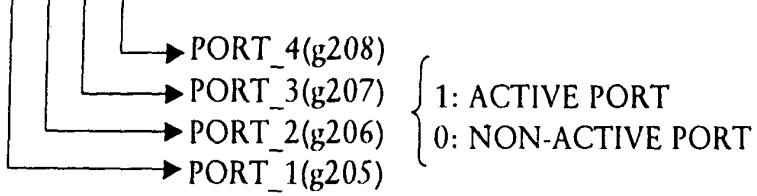


FIG.12

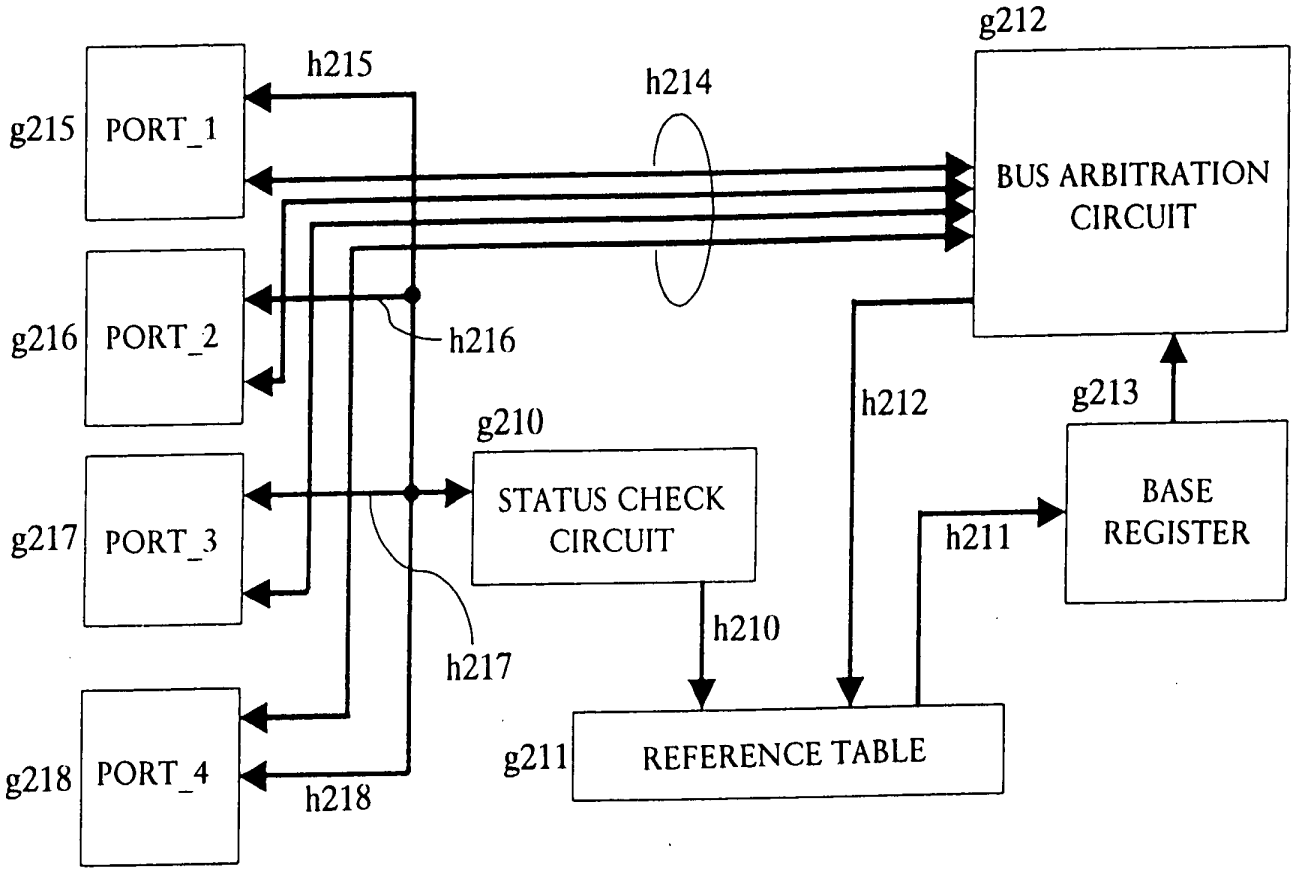

g212
h215
h214
g215
PORT_1
BUS ARBITRATION CIRCUIT
g216
PORT_2
h216
h212
g213
g210
STATUS CHECK CIRCUIT
BASE REGISTER
g217
PORT_3
h211
h210
h217
g218
PORT_4
g211
REFERENCE TABLE
h218

FIG.13

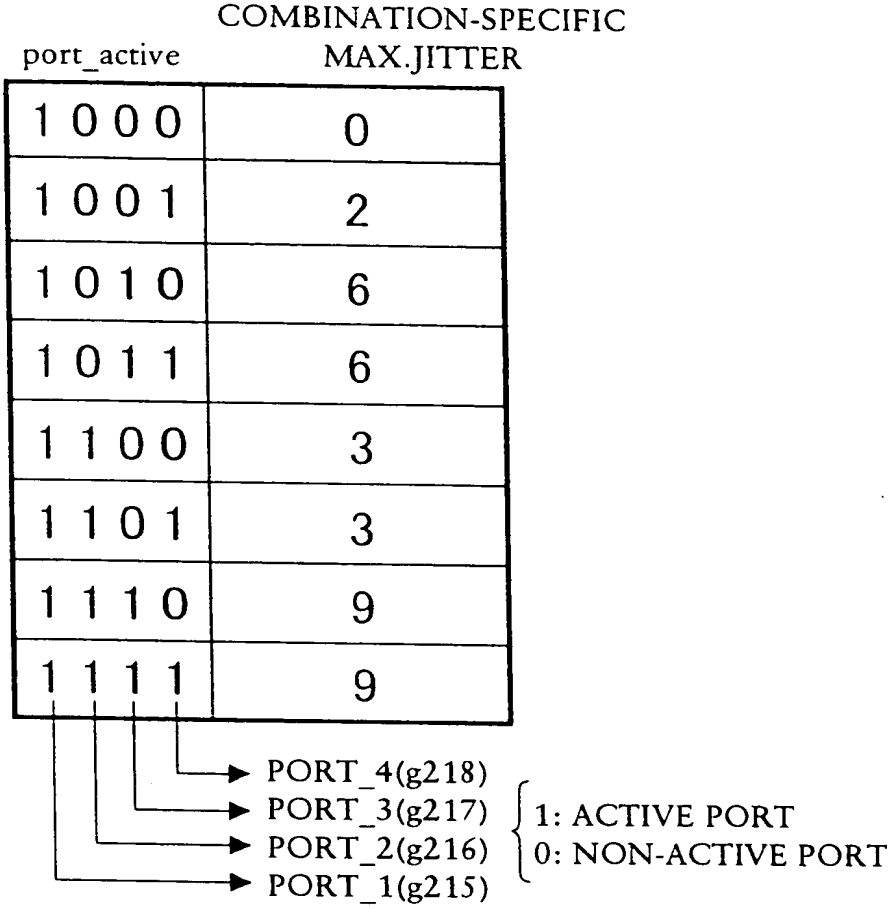

port_active
COMBINATION-SPECIFIC MAX.JITTER
1 0 0 0
0
1 0 0 1
2
1 0 1 0
6
1 0 1 1
6
1 1 0 0
3
1 1 0 1
3
1 1 1 0
9
1 1 1 1
9
PORT_4(g218)
PORT_3(g217)
PORT_2(g216)
PORT_1(g215)
1: ACTIVE PORT
0: NON-ACTIVE PORT

FIG.14

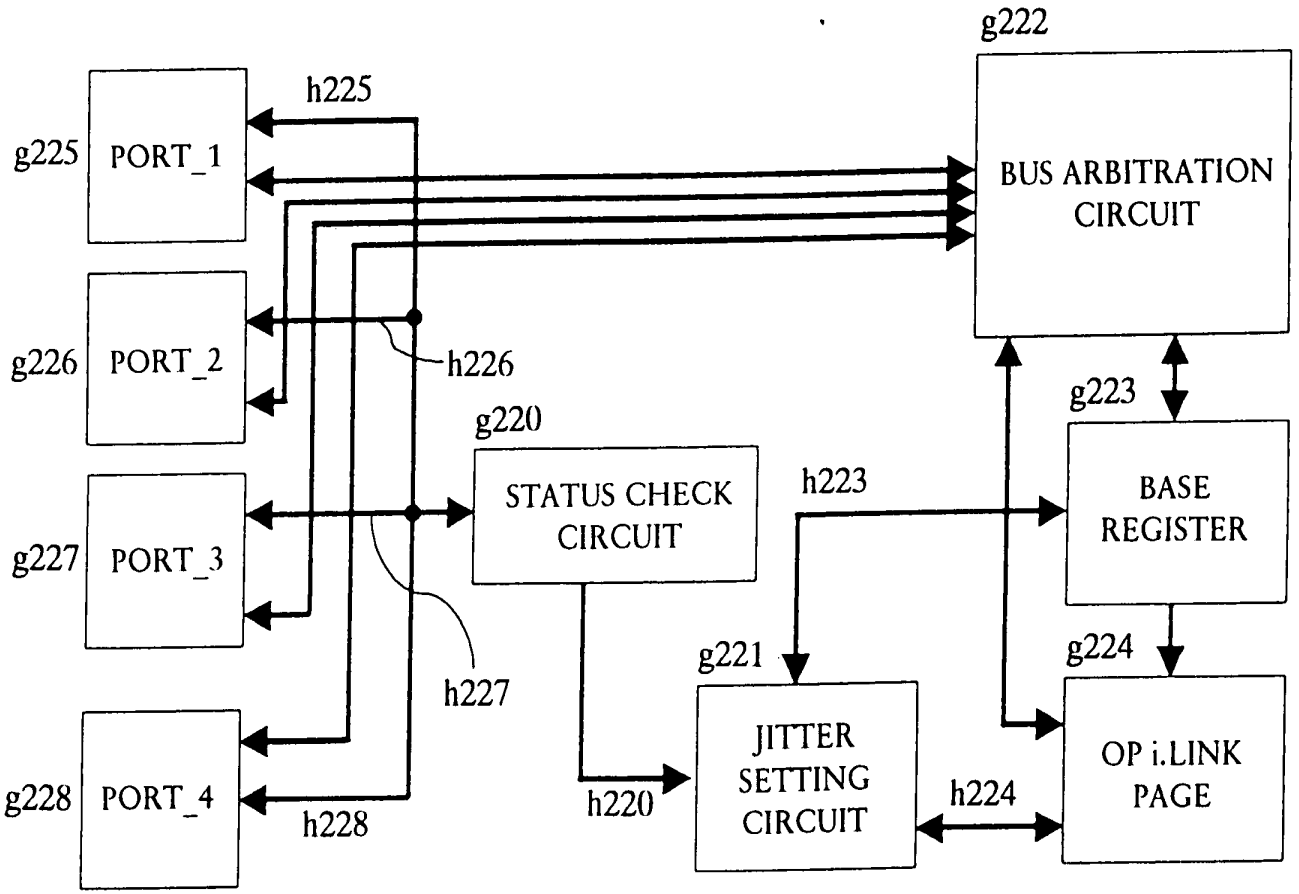

g222
BUS ARBITRATION CIRCUIT
h225
g225
PORT_1
g226
PORT_2
h226
g220
STATUS CHECK CIRCUIT
g223
BASE REGISTER
h223
g227
PORT_3
h227
g221
JITTER SETTING CIRCUIT
g224
OP i.LINK PAGE
g228
PORT_4
h228
h220
h224

FIG.15

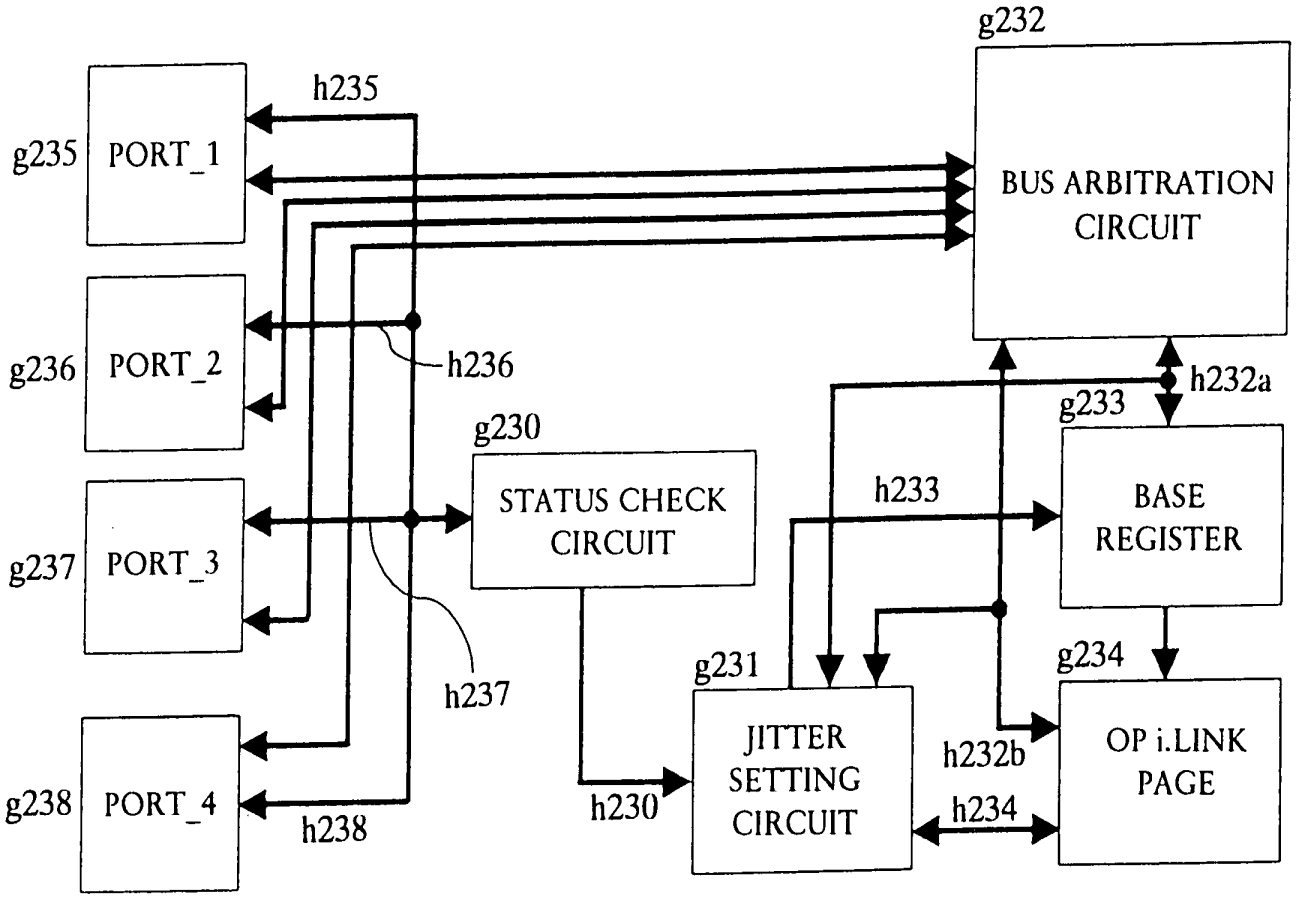

g232
BUS ARBITRATION CIRCUIT
h235
g235
PORT_1
g236
PORT_2
h236
h232a
g233
g230
STATUS CHECK CIRCUIT
h233
BASE REGISTER
g237
PORT_3
h237
g231
g234
JITTER SETTING CIRCUIT
h232b
OP i.LINK PAGE
g238
PORT_4
h238
h230
h234

FIG.16

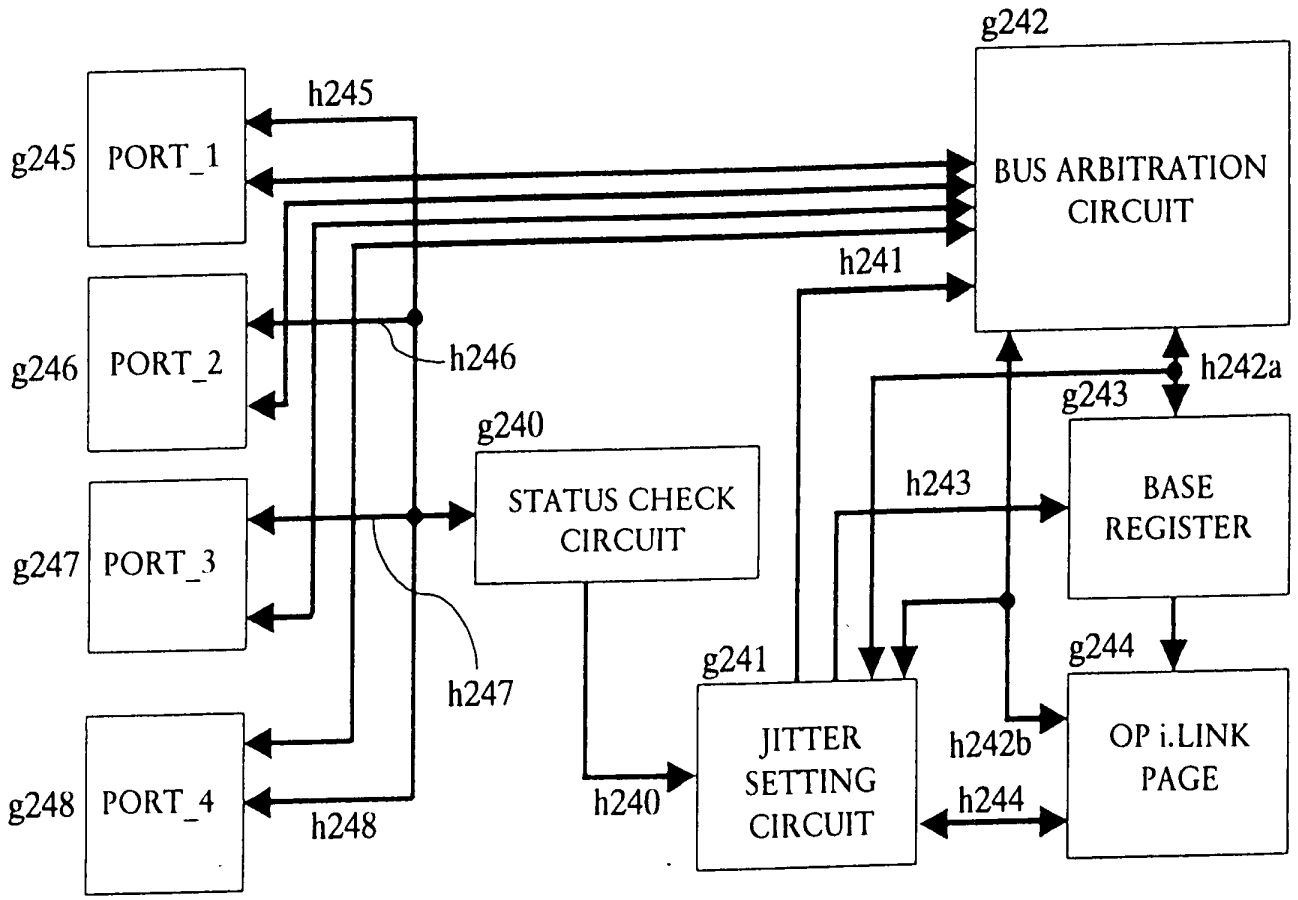

g242
BUS ARBITRATION CIRCUIT
h245
g245
PORT_1
h241
g246
PORT_2
h246
h242a
g243
g240
STATUS CHECK CIRCUIT
h243
BASE REGISTER
g247
PORT_3
g241
g244
h247
JITTER SETTING CIRCUIT
h242b
OP i.LINK PAGE
g248
PORT_4
h240
h244
h248

FIG.17

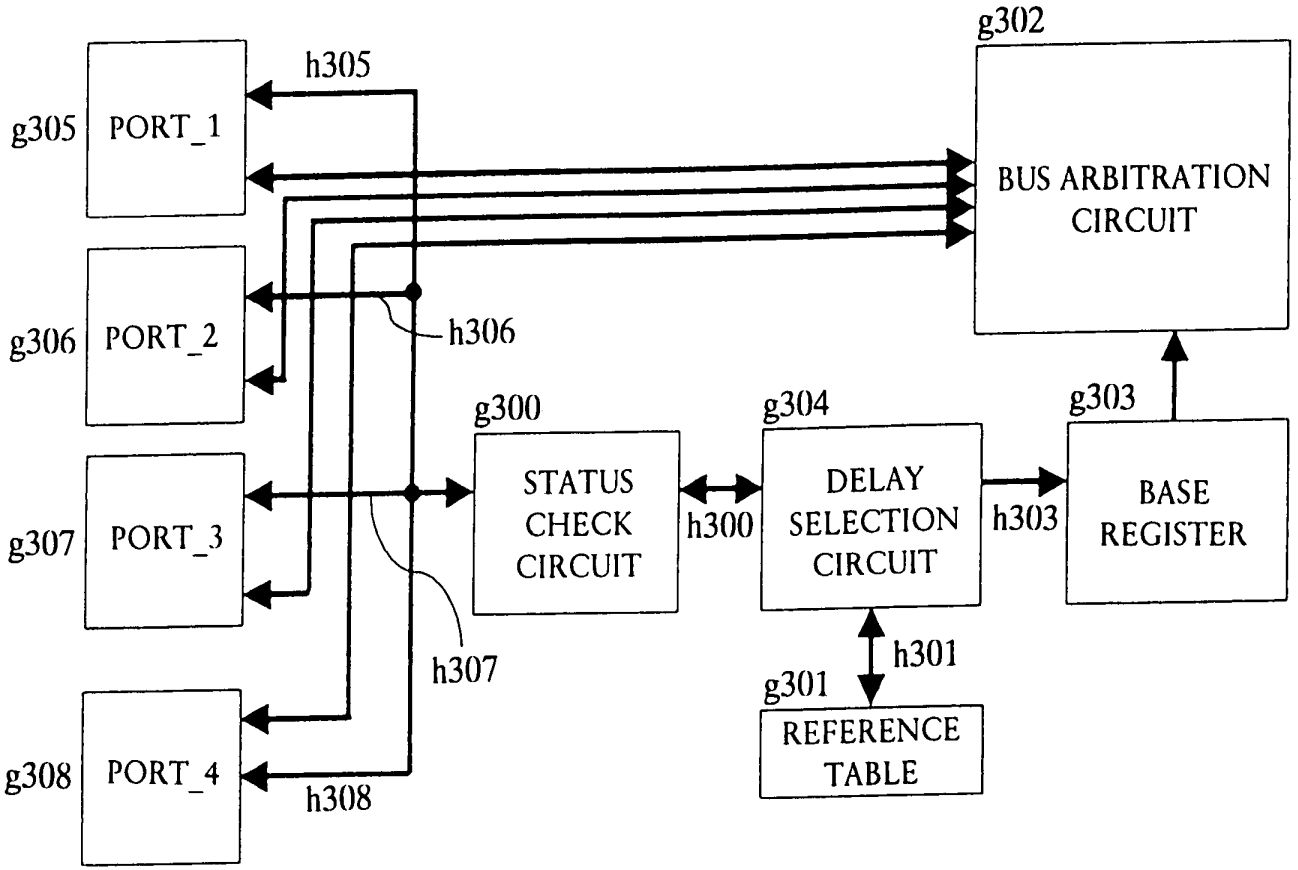

g302
BUS ARBITRATION CIRCUIT
h305
g305
PORT_1
g306
PORT_2
h306
g300
STATUS CHECK CIRCUIT
h300
g304
DELAY SELECTION CIRCUIT
h303
g303
BASE REGISTER
g307
PORT_3
h307
h301
g301
REFERENCE TABLE
g308
PORT_4
h308

FIG.18

	PORT_1 (g305)	PORT_2 (g306)	PORT_3 (g307)	PORT_4 (g308)
PORT_1 (g305)				
PORT_2 (g306)	3			
PORT_3 (g307)	6	9		
PORT_4 (g308)	2	5	8	

FIG.19

	PORT_1 (g305)	PORT_2 (g306)	PORT_3 (g307)	PORT_4 (g308)
PORT_1 (g305)	1			
PORT_2 (g306)	3	7		
PORT_3 (g307)	6	9	10	
PORT_4 (g308)	2	5	8	4

FIG.20

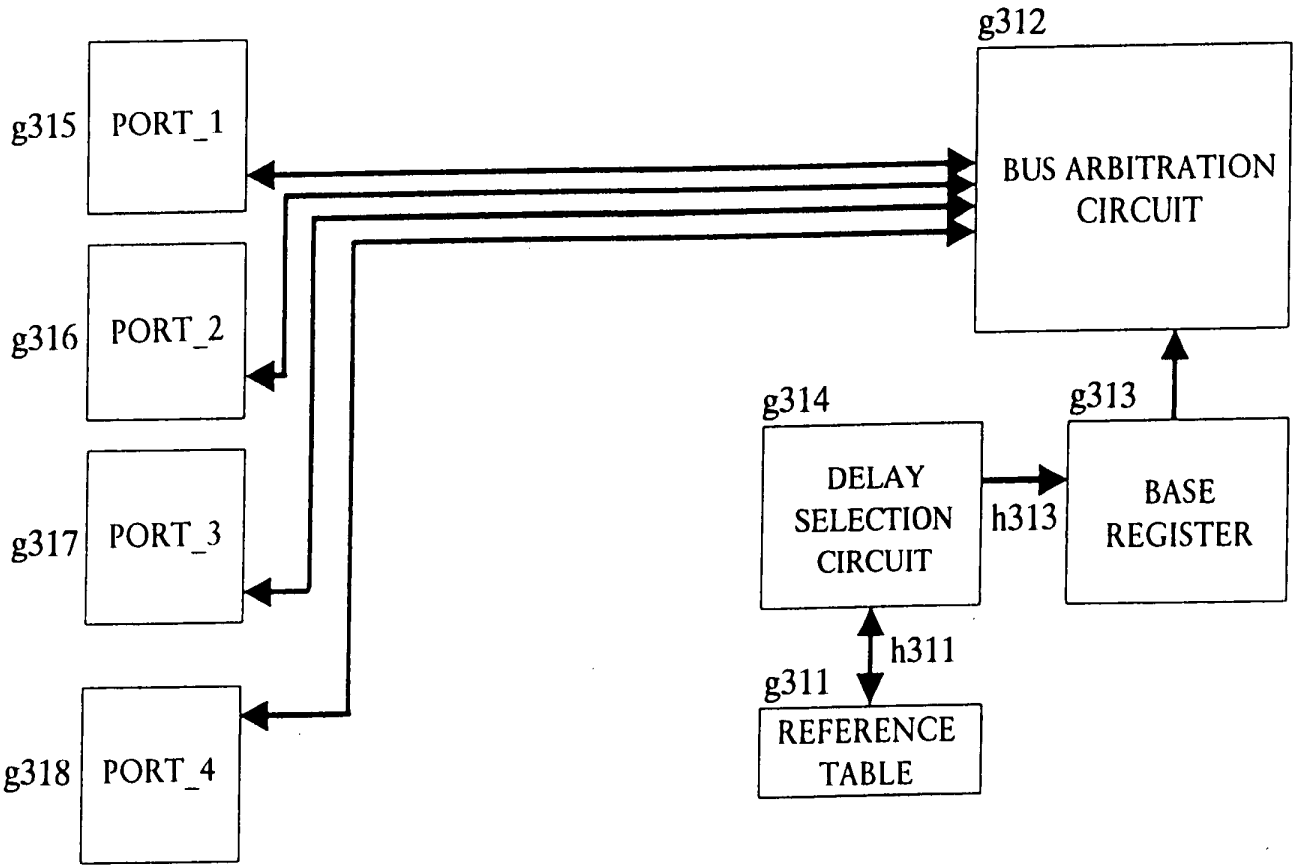

g312
BUS ARBITRATION CIRCUIT
g315
PORT_1
g316
PORT_2
g317
PORT_3
g318
PORT_4
g314
DELAY SELECTION CIRCUIT
h313
g313
BASE REGISTER
h311
g311
REFERENCE TABLE

FIG.21

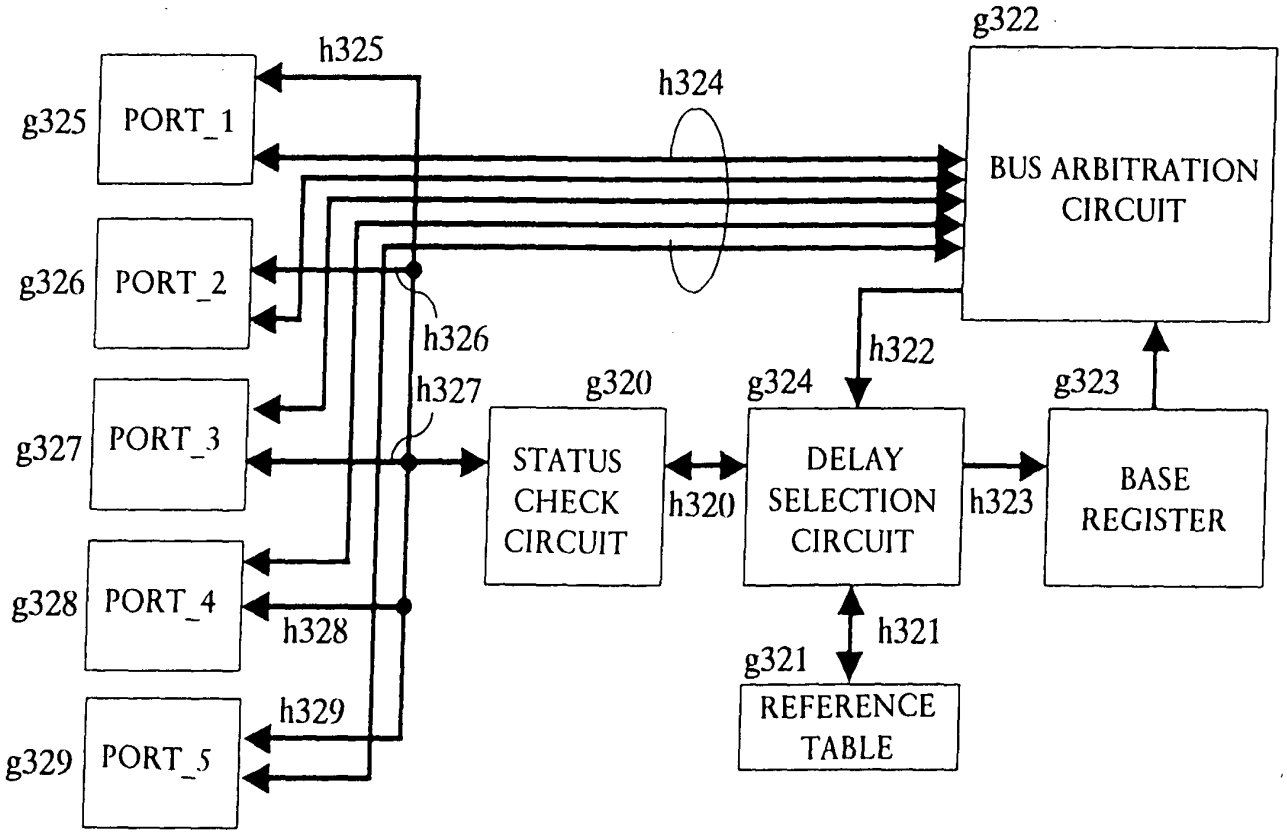

g322
h325
h324
g325
PORT_1
BUS ARBITRATION CIRCUIT
g326
PORT_2
h326
h322
h327
g320
g324
g323
g327
PORT_3
STATUS CHECK CIRCUIT
h320
DELAY SELECTION CIRCUIT
h323
BASE REGISTER
g328
PORT_4
h328
h321
g321
h329
REFERENCE TABLE
g329
PORT_5

FIG.22

	PORT_1 (g325)	PORT_2 (g326)	PORT_3 (g327)	PORT_4 (g328)	PORT_5 (g329)
PORT_1 (g325)	1				
PORT_2 (g326)	3	7			
PORT_3 (g327)	6	9	10		
PORT_4 (g328)	11	5	8	4	
PORT_5 (g329)	2	6	8	3	4

FIG.23

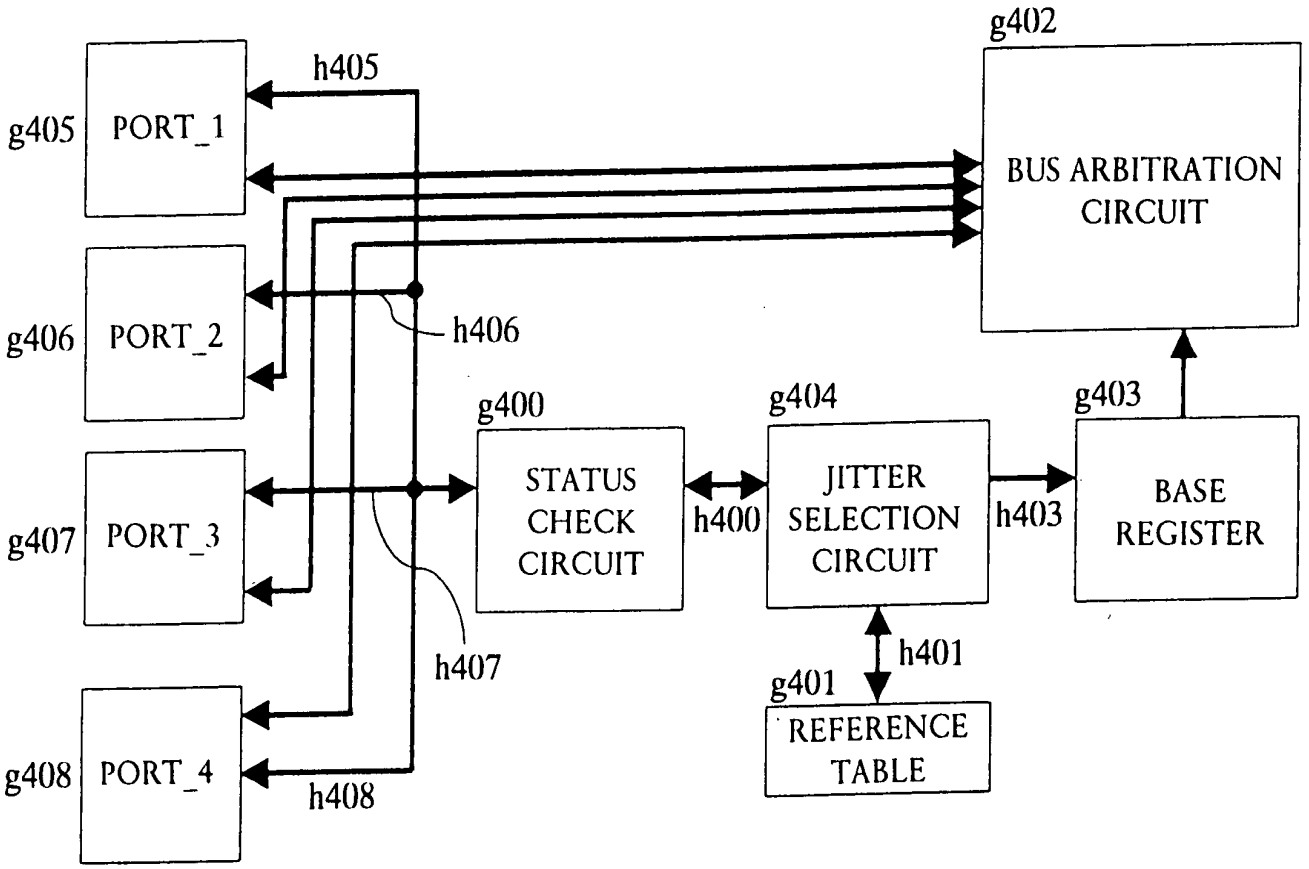

g402
h405
g405
PORT_1
BUS ARBITRATION CIRCUIT
g406
PORT_2
h406
g400
g404
g403
STATUS CHECK CIRCUIT
h400
JITTER SELECTION CIRCUIT
h403
BASE REGISTER
g407
PORT_3
h407
h401
g401
REFERENCE TABLE
g408
PORT_4
h408

FIG.24

	PORT_1 (g405)	PORT_2 (g406)	PORT_3 (g407)	PORT_4 (g408)
PORT_1 (g405)				
PORT_2 (g406)	3			
PORT_3 (g407)	6	9		
PORT_4 (g408)	2	5	8	

FIG.25

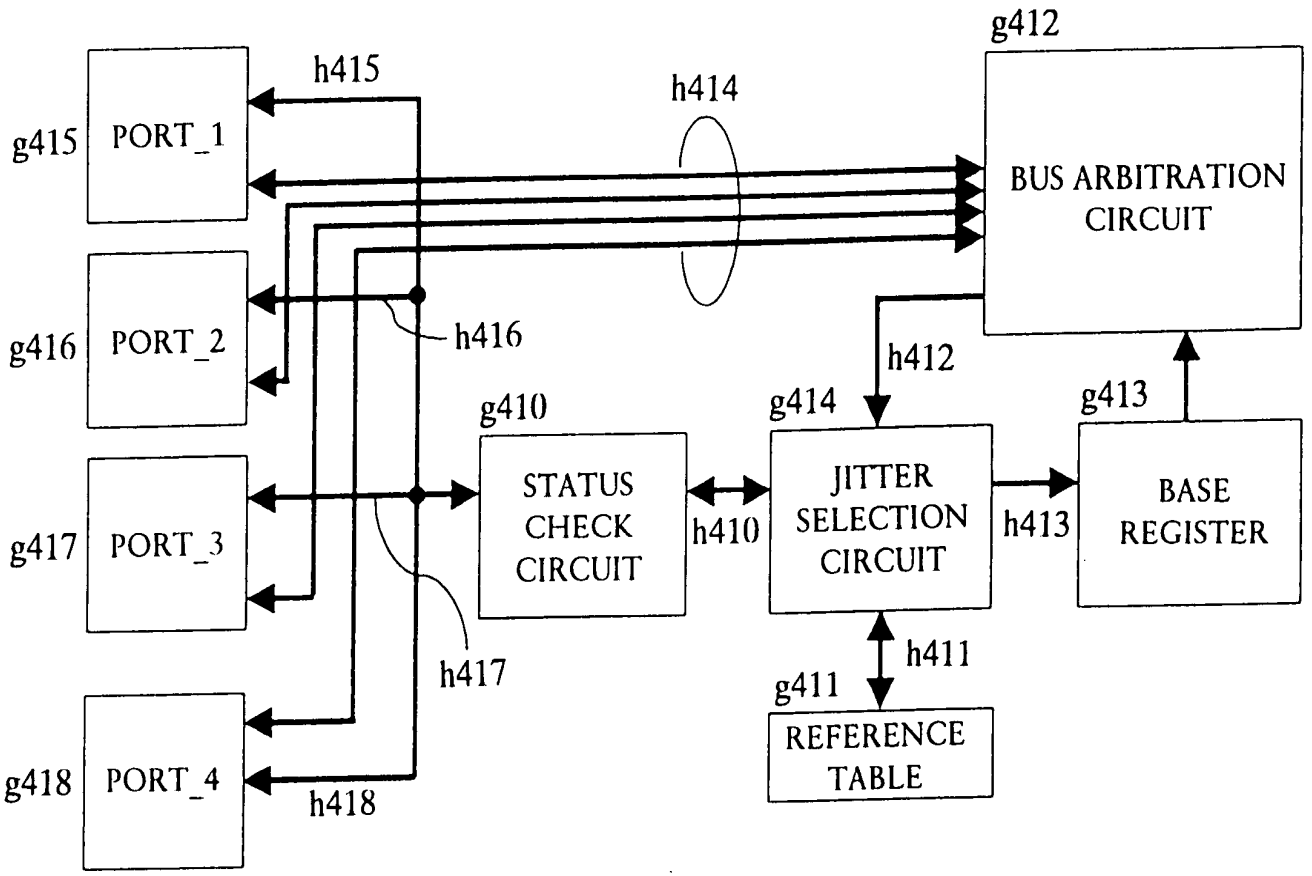

g412
h415
h414
g415
PORT_1
BUS ARBITRATION CIRCUIT
g416
PORT_2
h416
h412
g410
g414
g413
STATUS CHECK CIRCUIT
h410
JITTER SELECTION CIRCUIT
h413
BASE REGISTER
g417
PORT_3
h417
h411
g411
REFERENCE TABLE
g418
PORT_4
h418

FIG.26

	PORT_1 (g415)	PORT_2 (g416)	PORT_3 (g417)	PORT_4 (g418)
PORT_1 (g415)				
PORT_2 (g416)	3			
PORT_3 (g417)	6	9		
PORT_4 (g418)	2	5	8	

FIG.27

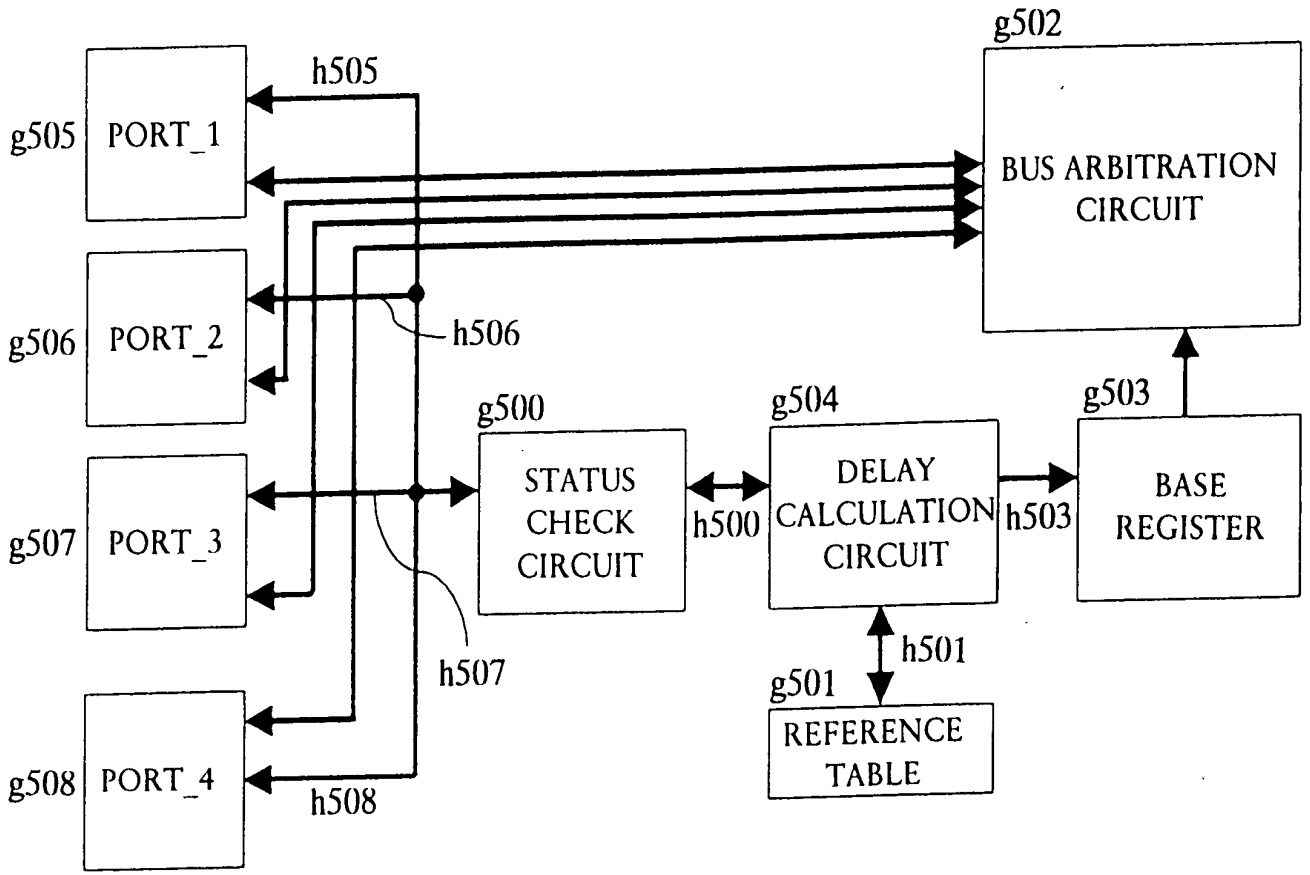

g502
BUS ARBITRATION CIRCUIT
h505
g505
PORT_1
g506
PORT_2
h506
g500
STATUS CHECK CIRCUIT
h500
g504
DELAY CALCULATION CIRCUIT
h503
g503
BASE REGISTER
g507
PORT_3
h507
h501
g501
REFERENCE TABLE
g508
PORT_4
h508

FIG.28

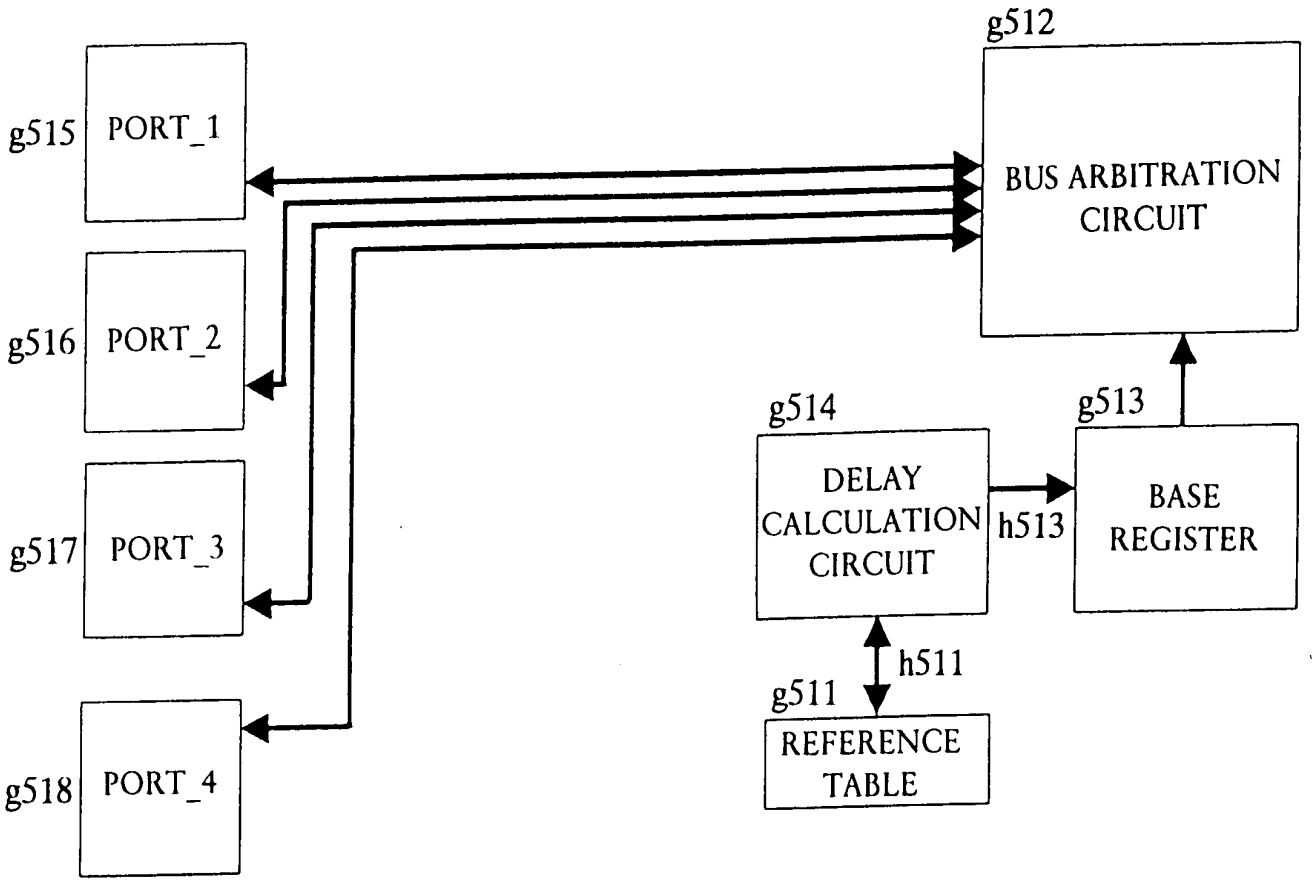

g512
BUS ARBITRATION CIRCUIT
g515
PORT_1
g516
PORT_2
g517
PORT_3
g518
PORT_4
g514
DELAY CALCULATION CIRCUIT
h513
g513
BASE REGISTER
h511
g511
REFERENCE TABLE

FIG.29

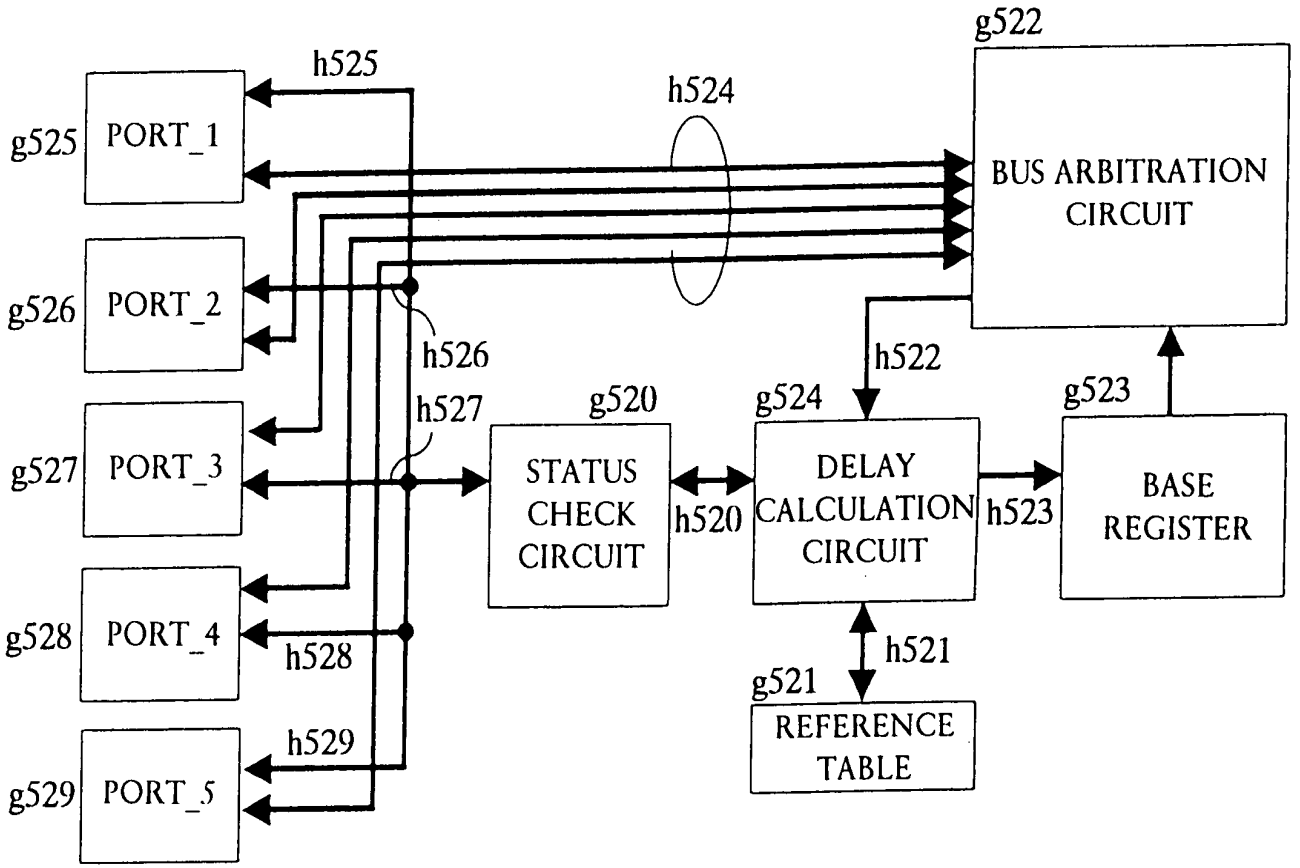

g522
h525
h524
g525
PORT_1
BUS ARBITRATION CIRCUIT
g526
PORT_2
h526
h522
h527
g520
g524
g523
g527
PORT_3
STATUS CHECK CIRCUIT
h520
DELAY CALCULATION CIRCUIT
h523
BASE REGISTER
g528
PORT_4
h528
h521
g521
h529
REFERENCE TABLE
g529
PORT_5

FIG.30

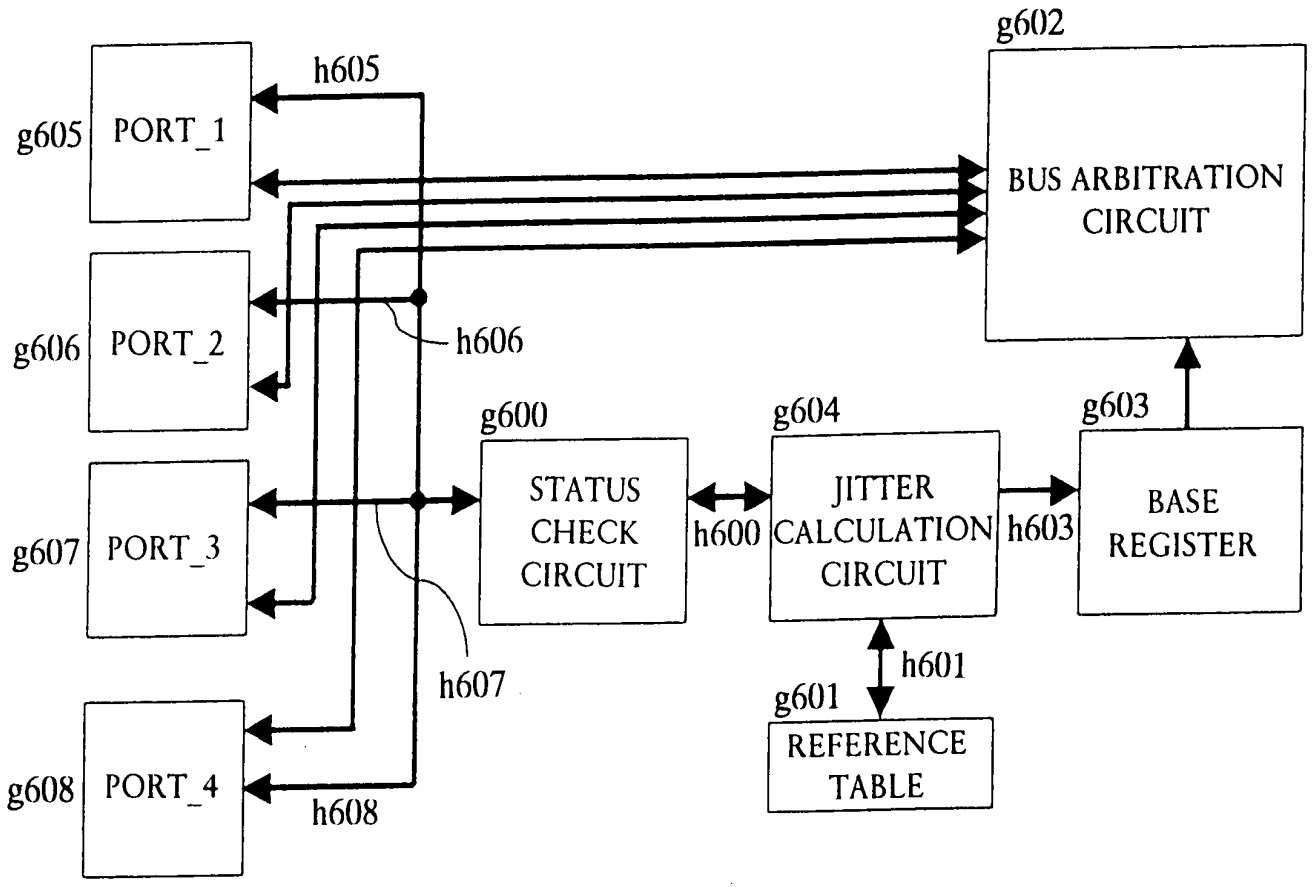

g602
BUS ARBITRATION CIRCUIT
h605
g605
PORT_1
g606
PORT_2
h606
g600
STATUS CHECK CIRCUIT
h600
g604
JITTER CALCULATION CIRCUIT
h603
g603
BASE REGISTER
g607
PORT_3
h607
h601
g601
REFERENCE TABLE
g608
PORT_4
h608

FIG.31

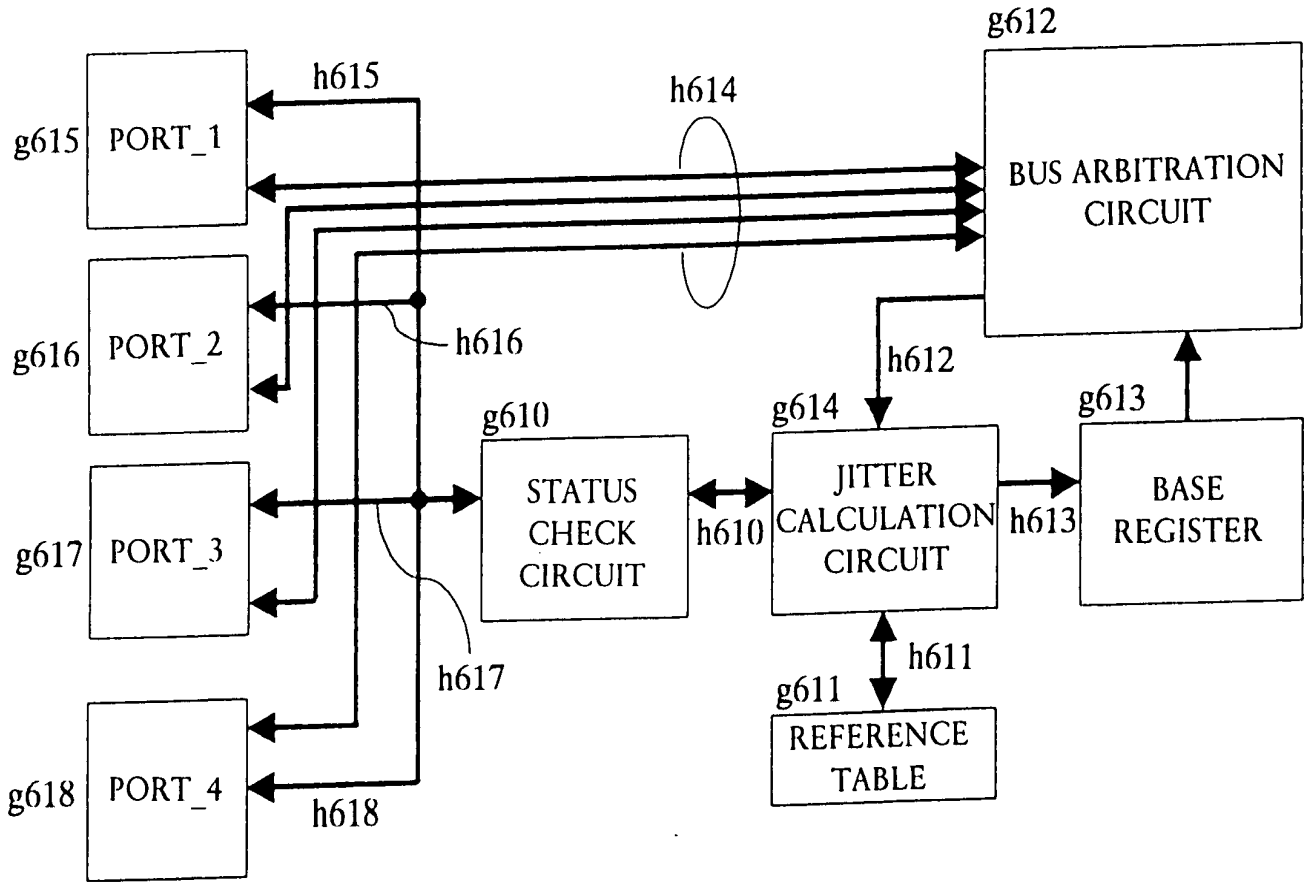

g612
h615
h614
g615
PORT_1
BUS ARBITRATION CIRCUIT
g616
PORT_2
h616
h612
g610
g614
g613
STATUS CHECK CIRCUIT
h610
JITTER CALCULATION CIRCUIT
h613
BASE REGISTER
g617
PORT_3
h617
h611
g611
REFERENCE TABLE
g618
PORT_4
h618

FIG.32

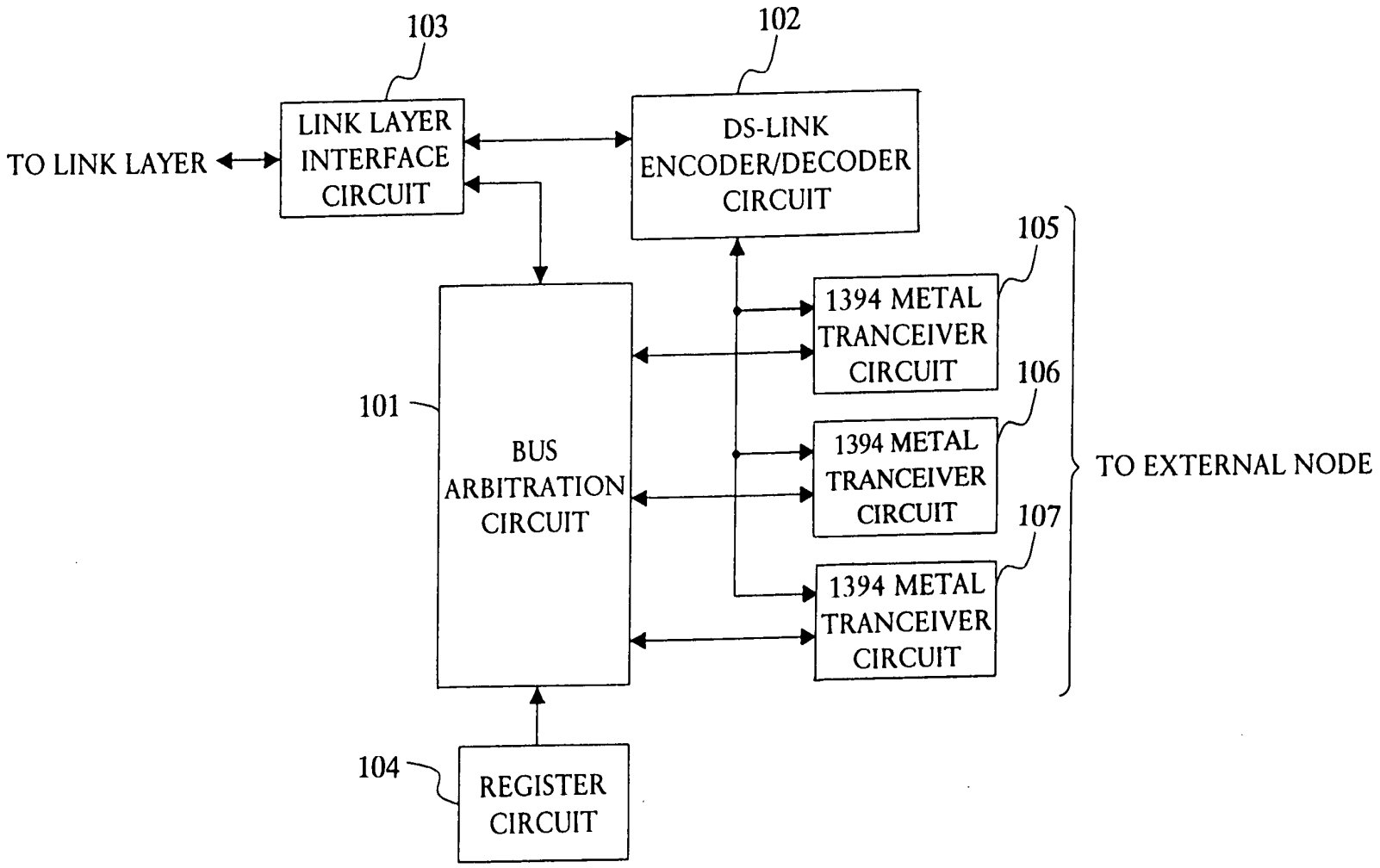

103
102
LINK LAYER INTERFACE CIRCUIT
TO LINK LAYER
DS-LINK ENCODER/DECODER CIRCUIT
105
1394 METAL TRANCEIVER CIRCUIT
106
1394 METAL TRANCEIVER CIRCUIT
107
1394 METAL TRANCEIVER CIRCUIT
TO EXTERNAL NODE
101
BUS ARBITRATION CIRCUIT
104
REGISTER CIRCUIT

FIG.33

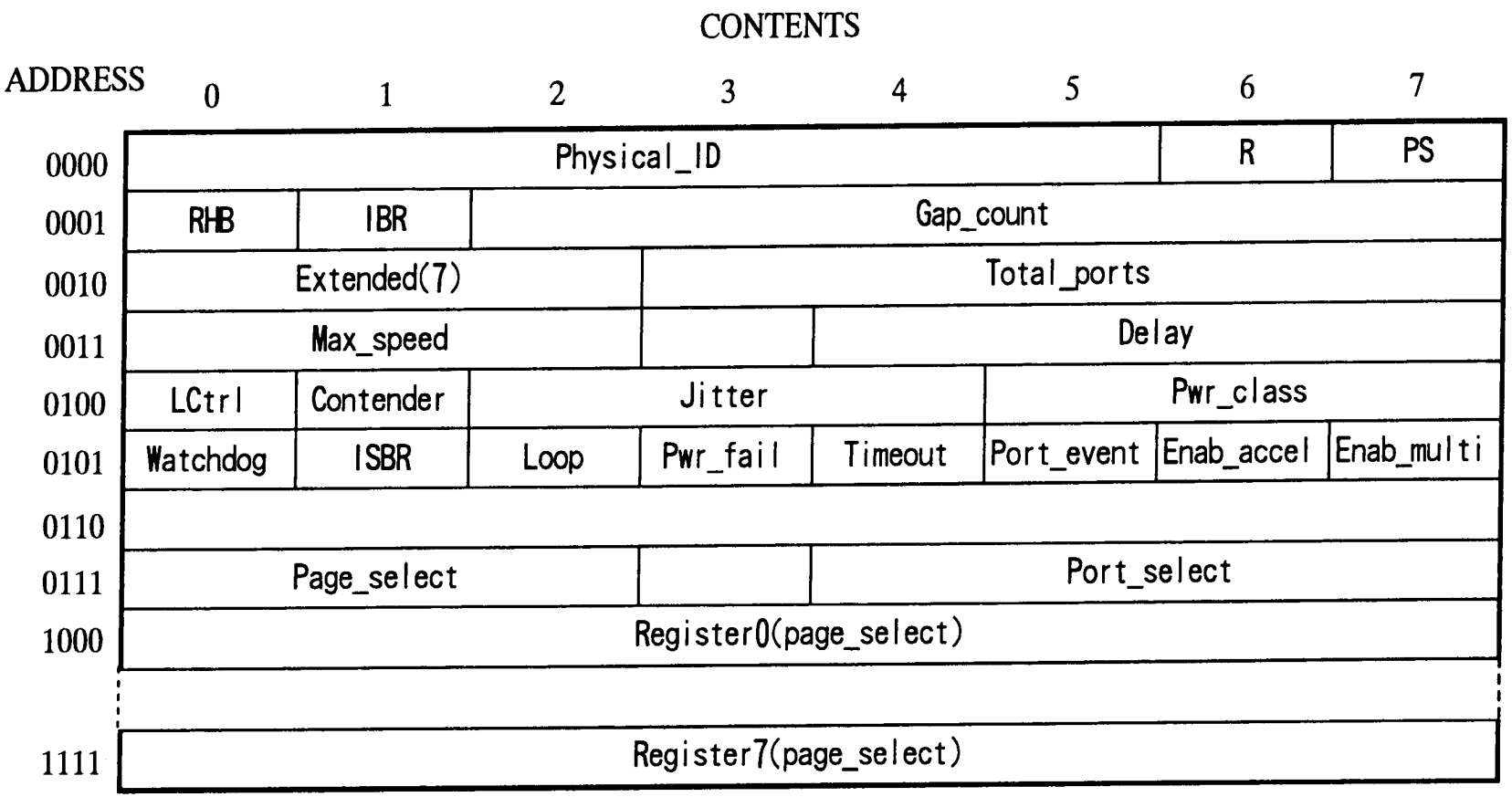

CONTENTS
ADDRESS
0
1
2
3
4
5
6
7
0000
Physical_ID
R
PS
0001
RHB
IBR
Gap_count
0010
Extended(7)
Total_ports
0011
Max_speed
Delay
0100
LCtrl
Contender
Jitter
Pwr_class
0101
Watchdog
ISBR
Loop
Pwr_fail
Timeout
Port_event
Enab_accel
Enab_multi
0110
0111
Page_select
Port_select
1000
Register0(page_select)
1111
Register7(page_select)

FIG.34

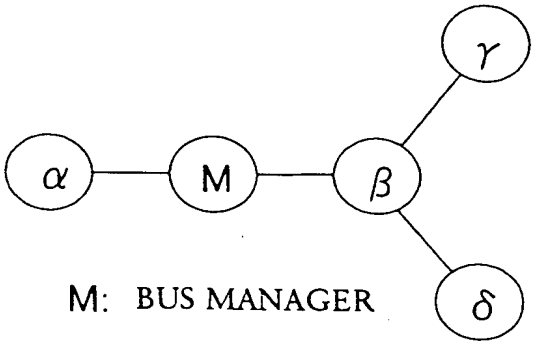
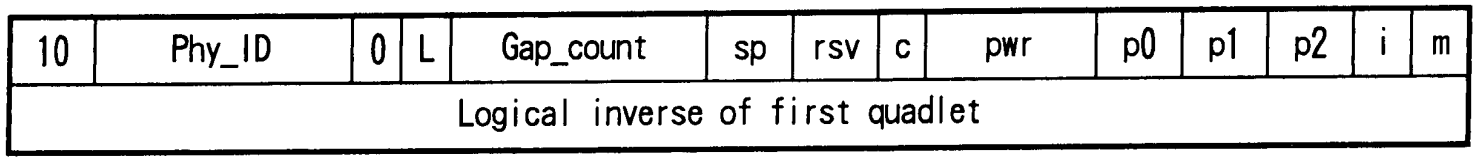


FIG.35

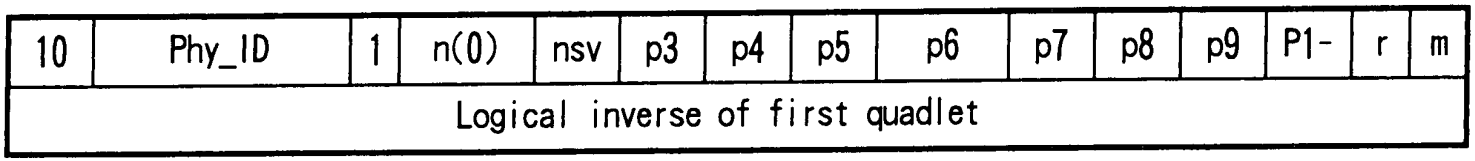
CONTENTS

ADDRESS	0	1	2	3	4	5	6	7
1000	4F							
1001	50							
1010	OP i.LINK version							
1011	Delay OP-DS				Jitter OP-DS			Pinging
1100	Delay DS-DS				Jitter DS-DS			
1101	T0	T1	T2	T3	T4	T5	T6	T7
1110	T8	T9	T10	T11	T12	T13	T14	T15
1111	Ping timer							

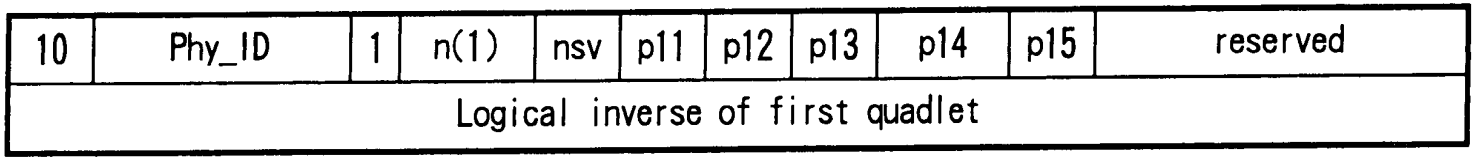
FIG.36



SELF ID PACKET #0



SELF ID PACKET #1



SELF ID PACKET #2

FIG.37

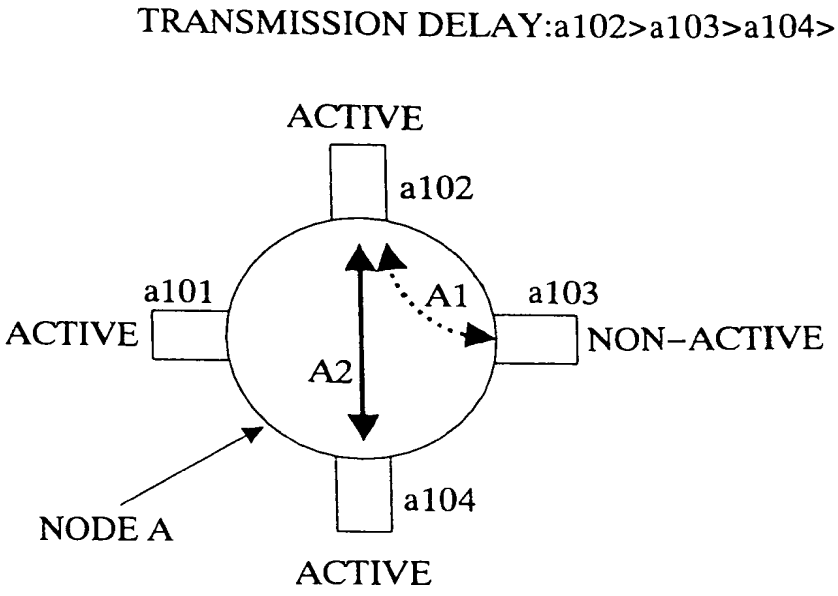

TRANSMISSION DELAY:a102>a103>a104>a101
ACTIVE
a102
a101
ACTIVE
A1
a103
NON-ACTIVE
A2
NODE A
a104
ACTIVE

FIG.38

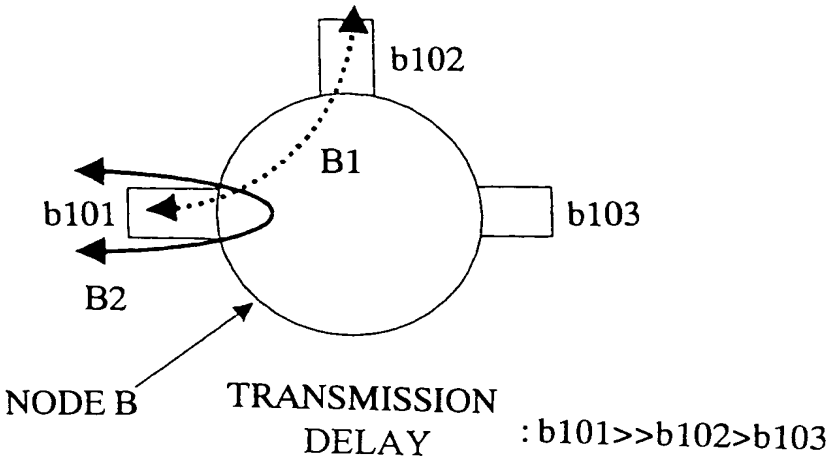

b102
B1
b101
b103
B2
NODE B
TRANSMISSION
DELAY
: b101>>b102>b103

FIG.39

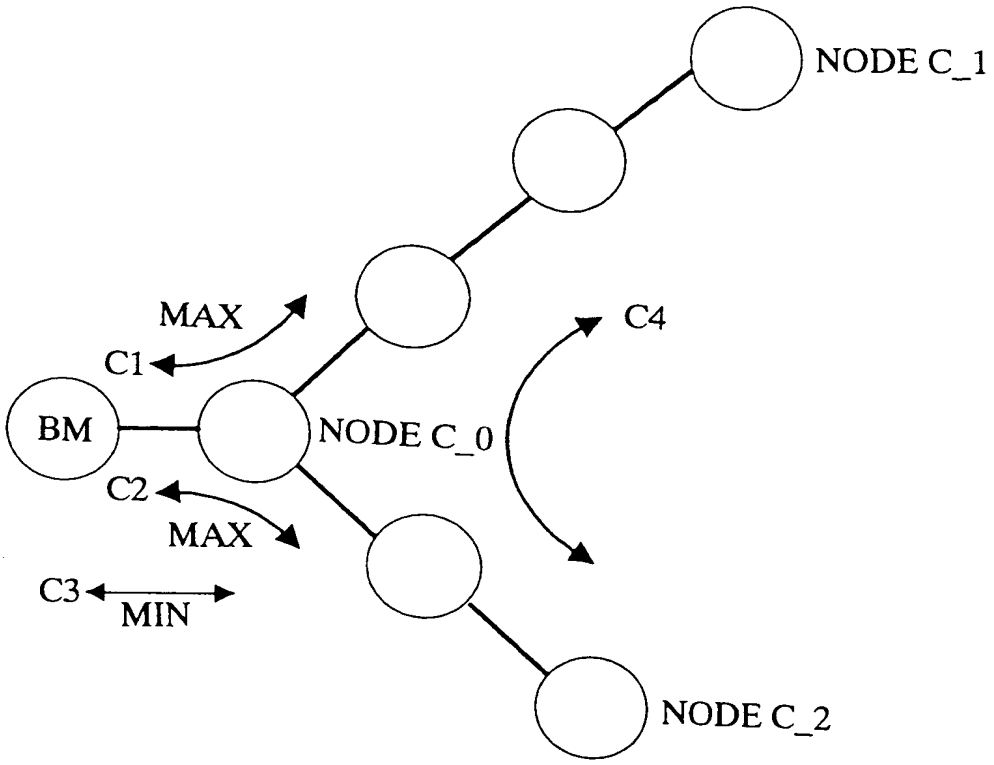


FIG.40

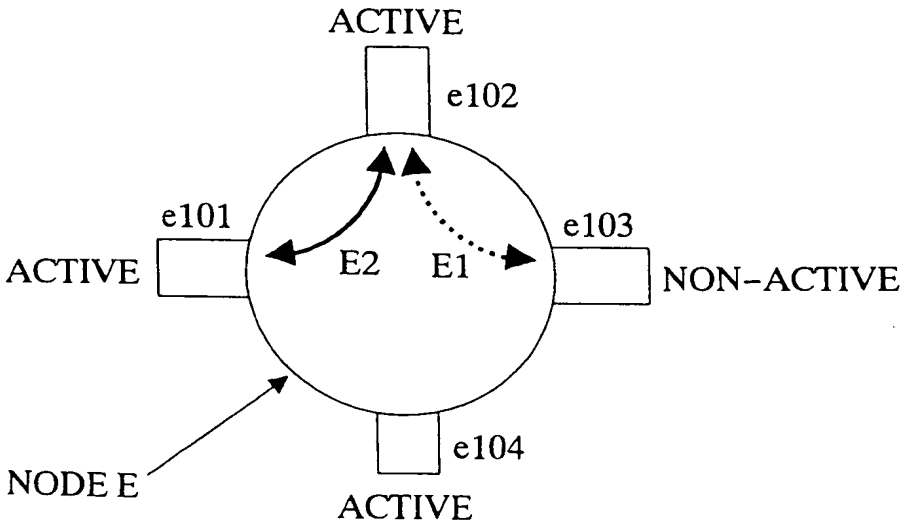
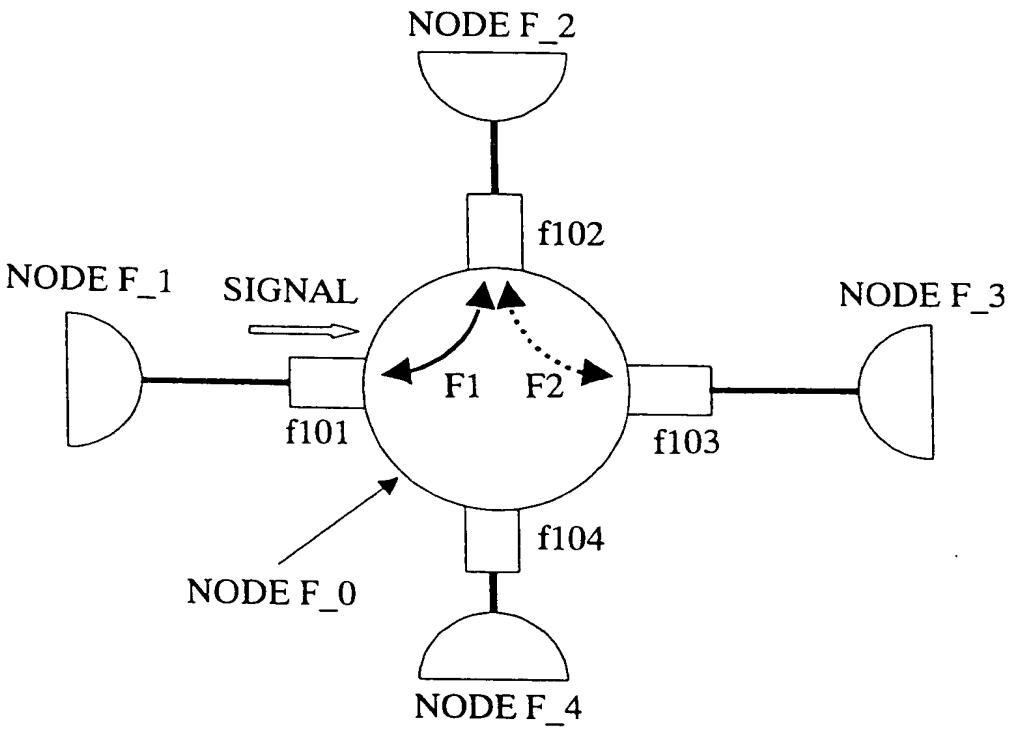

ACTIVE
e102
e101
ACTIVE
E2
E1
e103
NON-ACTIVE
NODE E
e104
ACTIVE

FIG.41


NODE F_2
f102
NODE F_1
SIGNAL
NODE F_3
F1
F2
f101
f103
f104
NODE F_0
NODE F_4